TMS320C6201
Test and Evaluation Board
Technical Reference

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Preface

Read This First

About This Manual

This manual describes the operation of the TMS320C6201 (’C6201) test and evaluation board (TEB). The ’C6201 TEB is a low-cost desktop card that helps you evaluate certain characteristics of the ’C6201 digital signal processor (DSP) to determine if the DSP meets your application requirements. You can create your software to run on the board and expand the system using the prototype area.

This manual tells you how to install and operate the ’C6201 TEB with your system. It also describes key features of the TEB and helps you understand the TEB’s key components.

How to Use This Manual

This book contains the following types of information:

- **Introductory material**, consisting of Chapters 1 and 2. Chapter 1 provides an overview of the ’C6201 TEB and its components. Chapter 2 tells you how to install the TEB.
- **Topical material**, consisting of Chapter 3, provides descriptions of hardware functions.
- **Reference material**, consisting of Appendixes A and B, provides PAL® code and schematics.

Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a `special typeface.`
- Device names are abbreviated with a C, followed by the last two to four alphanumeric characters in the name. For example, TMS320C6x is written as ’C6x and TMS320C6201 is written as ’C6201.

Information About Cautions

This book contains cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution is provided for your protection. Please read each caution carefully.

Related Documentation

You can use the following book to supplement this user's guide:

Programming Atmel's AT29 Flash Family, Flash Application Note (AN-3) (Atmel literature number 0518B)

Related Documentation From Texas Instruments

The following books describe the 'C6x devices and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When ordering, please identify the book by its title and literature number.

XDS51x Emulator Installation Guide (literature number SPNU070) describes the installation of the XDS510™, XDS510PP™, and XDS510WS™ emulator controllers. The installation of the XDS511™ emulator is also described.

JTAG/MPSD Emulation Technical Reference (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

TMS320C6x C Source Debugger User's Guide (literature number SPRU188) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

TMS320C6x C Source Debugger User's Guide (for SPARCstations) (literature number SPRU224) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface for SPARCstations. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

TMS320C62xx Technical Brief (literature number SPRU197) gives an introduction to the 'C62xx digital signal processor, development tools, and third-party support.

TMS320C6201 Digital Signal Processor Data Sheet (literature number SPRS051) describes the features of the TMS320C6xx and provides pinouts, electrical specifications, and timings for the device.

TMS320C62xx Peripherals Reference Guide (literature number SPRU190) describes common peripherals available on the TMS320C62xx digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

TMS320C62xx CPU and Instruction Set Reference Guide (literature number SPRU189) describes the 'C62xx CPU architecture, instruction set, pipeline, and interrupts for the TMS320C62xx digital signal processors.

TMS320C62xx Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code and includes application program examples.

TMS320C6x Optimizing C Compiler User's Guide (literature number SPRU187) describes the 'C6x C compiler. This C compiler accepts ANSI standard C source code and produces assembly language source code for the 'C6x generation of devices. This book also describes the assembly optimizer, which helps you optimize your assembly code.

TMS320C6x Assembly Language Tools User's Guide (literature number SPRU186) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the 'C6x generation of devices.

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Chapter 1

Overview of the TMS320C6201 Test and Evaluation Board

The TMS320C6201 test and evaluation board (TEB) helps you evaluate certain characteristics of the TMS320C6201 ('C6201) fixed-point digital signal processor (DSP) to ensure that it meets your application requirements. The TEB is self-contained, only requiring connections to an AC power supply and to your own emulation hardware and software. The TEB is platform independent and uses either an XDS510™ emulator controller for a PC™ or an XDS510WS™ emulator controller for a UNIX™ workstation.

The 'C6201 TEB carries a 'C6201 DSP on board to allow full-speed verification of 'C6201 code. You can also use the TEB to design your own prototype systems. The 'C6201 DSP has 128 Kbyte on-chip SRAM that consists of 64 Kbyte internal program/cache and 64 Kbyte internal data memory. The TEB uses the 'C6201's 32-bit external memory interface to facilitate accesses to on-board synchronous and asynchronous memories. A PC or UNIX windows-oriented debugger simplifies code development and debugging. For more information about the debugger, see the *TMS320C6201 C Source Debugger User's Guide* or the *TMS320C6x C Source Debugger User's Guide for SPARCStation*.

The TEB also has a 'C6201 16-bit host access port, a serial and timer access port, an IEEE Standard 1149.1-compliant JTAG connector for accessing the 'C6201's scan-based emulation features, and a through-hole area for design prototyping. You can also use the TEB as a reference when designing your own systems.

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1.1 Key Features of the TMS320C6201 TEB

The ’C6201 TEB has the following features:

- ’C6201 capable of executing 1600 million instructions per second (MIPS)
- Varied instruction cycle times of the ’C6201:
  - 5-ns instruction cycle time when using the DSP’s internal memories
  - 6-ns instruction cycle time when using synchronous dynamic RAM (SDRAM) and one-half rate external synchronous burst static RAM (SBSRAM)
  - 6.7-ns instruction cycle time when using the TEB’s external SBSRAM, regardless of which other TEB memories are used
- 512K bytes 6.7-ns SBSRAM
- 8M bytes 12-ns SDRAM
- 256K bytes 12-ns asynchronous static RAM (ASRAM)
- 128K bytes 200-ns flash programmable erasable ROM (PEROM)
- 16-bit host port header
- Access to the ’C6201’s serial ports and timers via a header
- Emulator connector
- Prototyping area

1.2 Functional Overview of the TMS320C6201 TEB

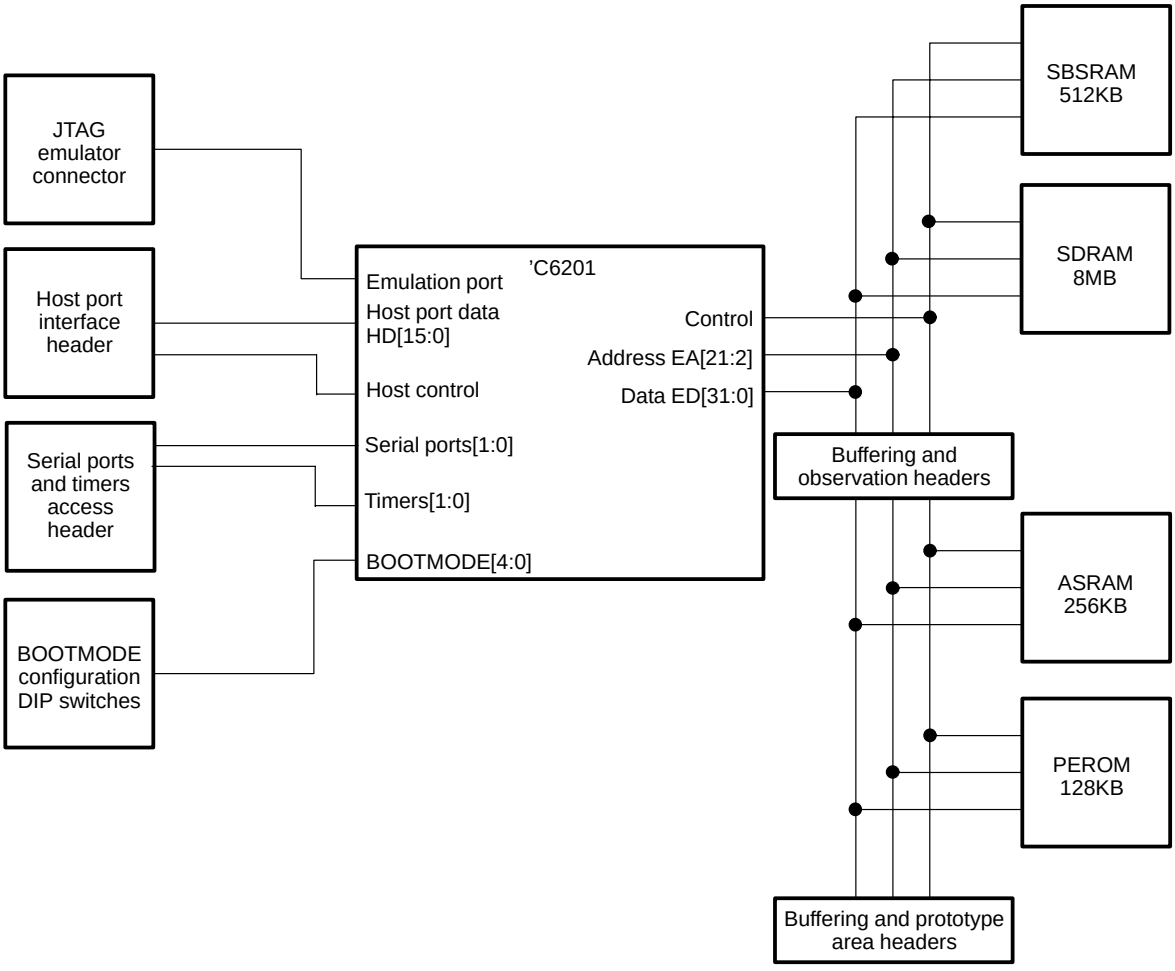
Figure 1–1 shows the basic block diagram and interconnects of the ’C6201 TEB. The interconnects include the external memory, host port, emulation interfaces, and serial ports and timers.

The ’C6201 DSP interfaces to the memories through a 32-bit data bus. Headers are situated between the synchronous and asynchronous memories to allow easy examination of the external memory interface’s address, data, and control signals. The TEB’s control signals are also available at these headers. Additional headers between the asynchronous memories and the prototyping area allow for access to asynchronous control signals and the data bus, which may be used in the prototyping area.

Use the host port header to connect your host processor to the ’C6201’s host port interface. This allows your host processor to access the ’C6201’s internal memory. The serial ports and timers header allows access to the ’C6201’s serial ports and timers.

An emulation connector provides access to the IEEE Standard 1149.1 (JTAG) scan-based emulation port of the ’C6201. This port is a superset of the IEEE 1149.1 standard and is used by either an XDS510 or an XDS510WS emulator.

Figure 1–1. TMS320C6201 TEB Connectivity



Chapter 2

Installing the TMS320C6201 Test and Evaluation Board

This chapter provides installation instructions for the ’C6201 TEB.

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2.1 The TMS320C6201 TEB

The ’C6201 TEB is 5 inches x 12 inches and is intended for desktop use. It meets the following specifications:

- Instruction cycles of 7.5 ns (frequency equal to 133 MHz). This is accomplished using a 33.25-MHz oscillator and operating the ’C6201’s phase-locked loop (PLL) clock in multiply-by-four mode.
- Configuration of the ’C6201 boot process using the TEB’s on-board DIP switches. These switches are set for the following:
  - Use of the ’C6201’s memory map 1
  - Memory at address 0 is ’C6201 internal RAM
  - Boot-load startup process using 8-bit PEROM with default timing in CE1 external address space
- Use of the emulator’s TCLK signal

Figure 2–1 shows the layout of the ’C6201 TEB.

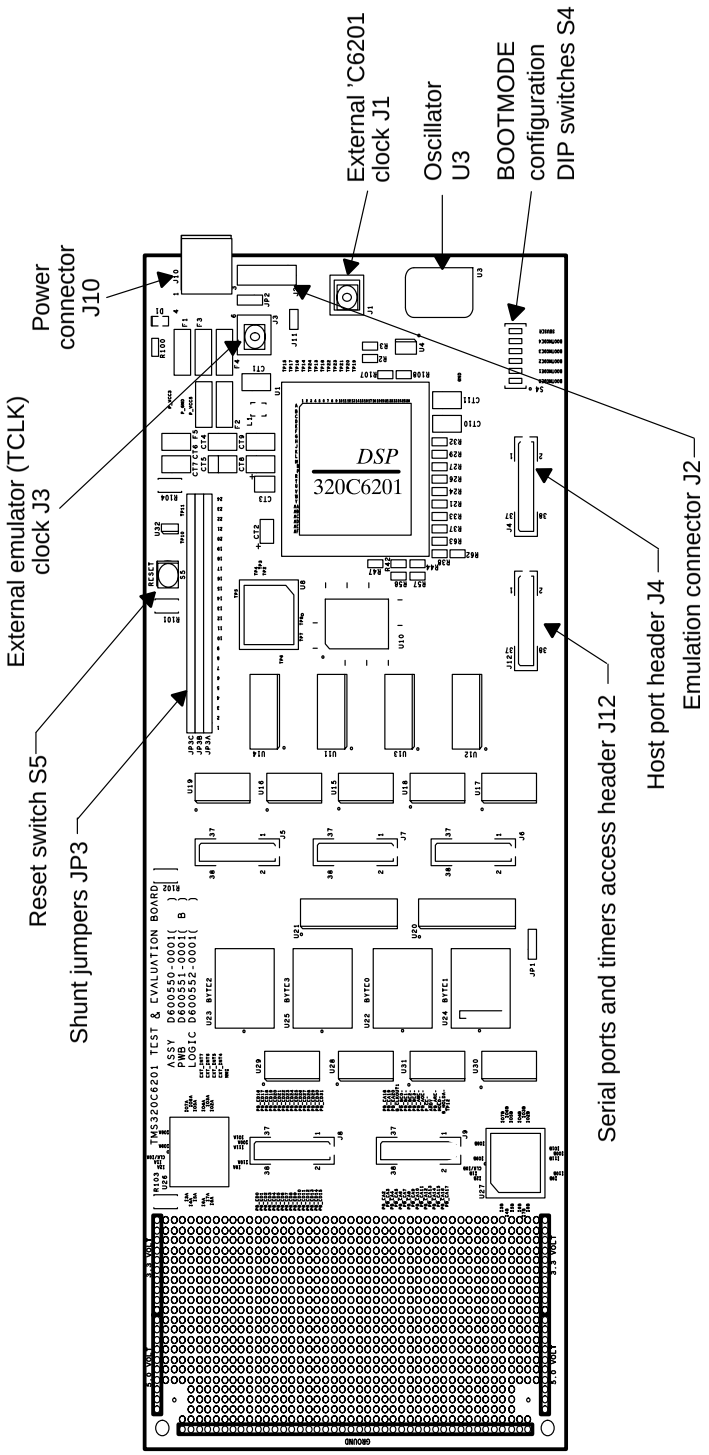


Figure 2–1. TMS320C6201 TEB

2.2 Host Requirements

The TEB is platform independent and can be used with an XDS510 emulator controller for a PC or an XDS510WS emulator controller for a UNIX workstation. The *XDS51x Emulator Installation Guide* lists the minimum hardware requirements for your emulator. The installation instructions included with your emulator software lists the minimum software requirements for your emulator.

2.3 TMS320C6201 TEB Kit Components

The kit contains the following items:

- ❑ 'C6201 TEB
- ❑ Custom power supply
- ❑ *TMS320C6201 Test and Evaluation Board Technical Reference* (this document)
- ❑ Diskette containing TEB-related files

2.4 TMS320C6201 TEB Connection

Before you apply power to the TEB or connect the TEB to your emulator, see Table 2–1 and Table 2–2 to ensure that all shunt jumpers and DIP switches are set to their default positions. Table 3–3 and Table 3–4 contain complete descriptions of all shunt jumpers and DIP switches used on the TEB. See these tables before you change any default settings.

Table 2–1. Default TEB Shunt Jumper Settings

A–B indicates HIGH (1), B–C indicates LOW (0)

Name	Position	Setting	Description
ROM protect	JP1	1–2	Flash PEROM write disabled
TCLK select	JP2	2–3	Use XDS51x emulator's TCLK signal
NMI	JP3.1	B–C	Nonmaskable interrupt inactive
EXT_INT4	JP3.2	B–C	Interrupts EXT_INT4—EXT_INT7 inactive
EXT_INT5	JP3.3	B–C	
EXT_INT6	JP3.4	B–C	
EXT_INT7	JP3.5	B–C	
PLLFREQ1	JP3.6	B–C	25 MHz < CLKOUT1 ≤ 135 MHz
PLLFREQ2	JP3.7	B–C	
PLLFREQ3	JP3.8	B–C	
CLKMODE0	JP3.9	A–B	PLL multiply-by-four mode
CLKMODE1	JP3.10	A–B	
RSV0	JP3.11	A–B	Reserved
RSV1	JP3.12	A–B	
RSV2	JP3.13	A–B	
RSV3	JP3.14	A–B	
RSV4	JP3.15	B–C	
EMU0	JP3.16	A–B	TI emulation support
EMU1	JP3.17	A–B	
LENDIAN	JP3.18	A–B	Little-endian mode addressing
ARDY	JP3.19	A–B	External controller ready (to avoid stalling)
HOLD–	JP3.20	A–B	Connects 'C6201 to the system
Unused	JP3.21	No Shunt	
Unused	JP3.22	No Shunt	
TINP0	JP3.23	A–B	Timer inputs
TINP1	JP3.24	A–B	

Table 2–2. Default TEB DIP Switch Settings

OFF indicates HIGH (1), ON indicates LOW (0)

Name	Position	Setting	Description
BOOTMODE0	S4.1	OFF	Boot configuration settings for memory map 1 with internal RAM at address 0 and 8-bit PEROM boot process
BOOTMODE1	S4.2	ON	
BOOTMODE2	S4.3	OFF	
BOOTMODE3	S4.4	OFF	
BOOTMODE4	S4.5	ON	
SWUSER	S4.6	OFF	User-defined input to U8 PAL®

2.5 TMS320C6201 TEB Installation

The ’C6201 TEB is connected to a power supply and an emulator. The following steps show how to connect the TEB to both.

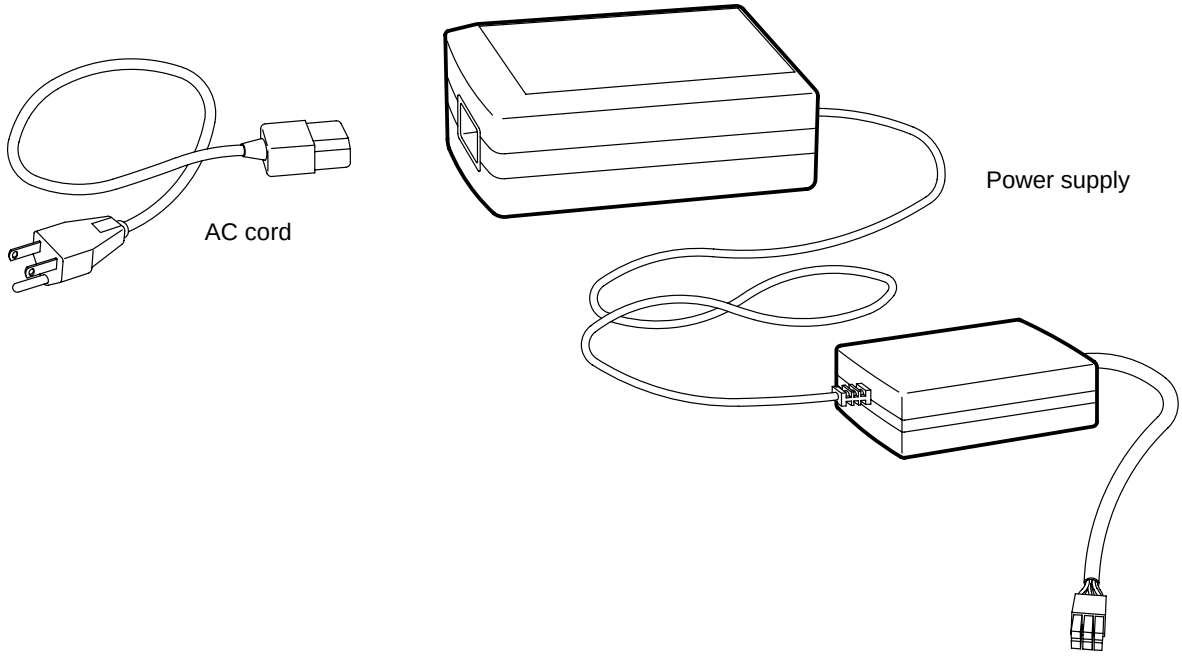
Never disconnect or reconnect any cables or other hardware devices while power is applied to the emulator or TEB. Doing so can cause damage to your emulator and/or TEB.

Step 1: Install your emulation hardware and software.

Step 2: Ensure the emulator power is off. If you have an XDS510WS emulator controller (for a UNIX workstation), switch off the power. If you have an XDS510 emulator controller (for a PC), power down the emulator by shutting down Windows and turning off your PC.

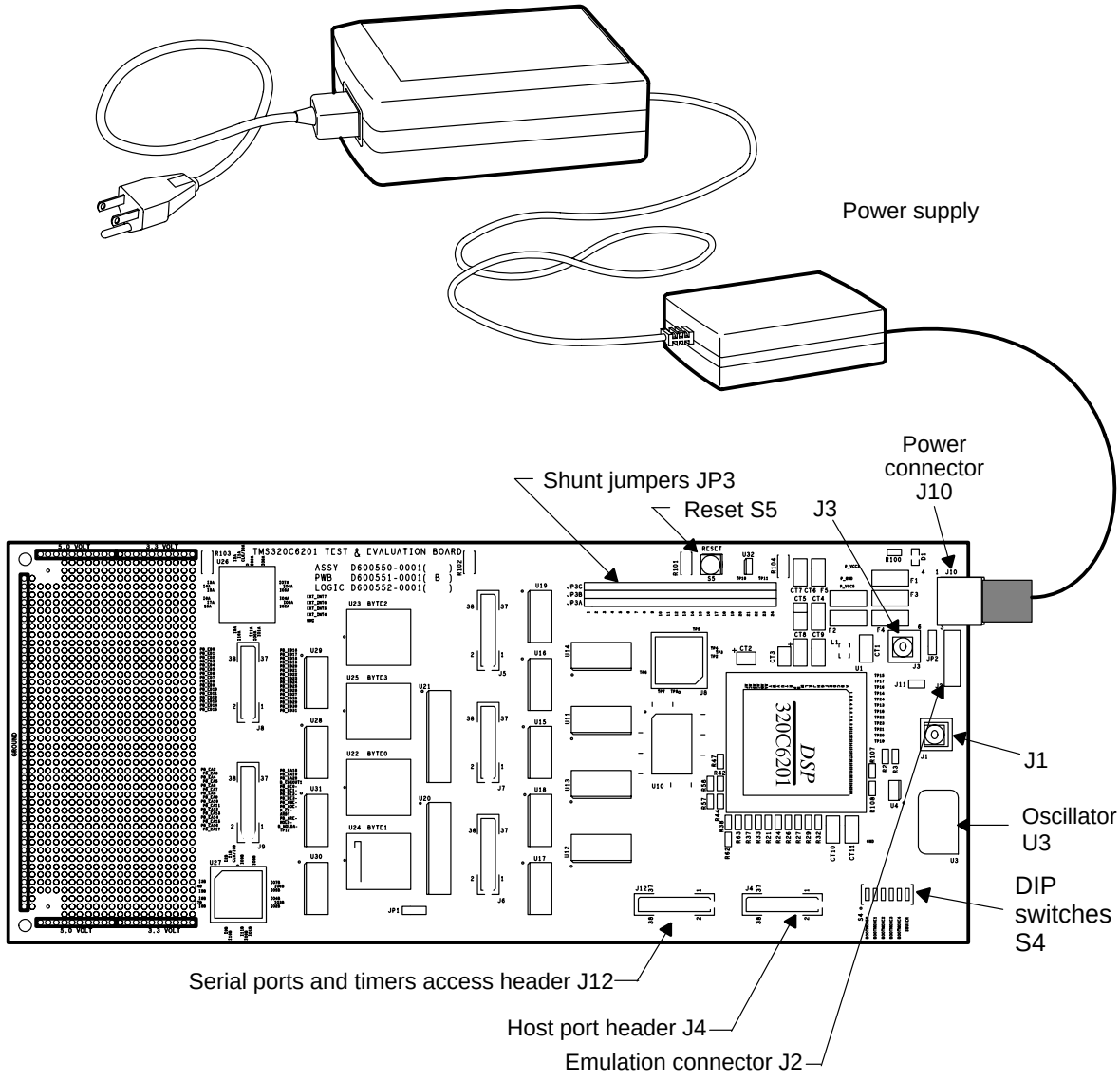
Step 3: Insert the female end of the AC line cord into the power supply.

Figure 2–2. Attaching AC Cord Into Power Supply



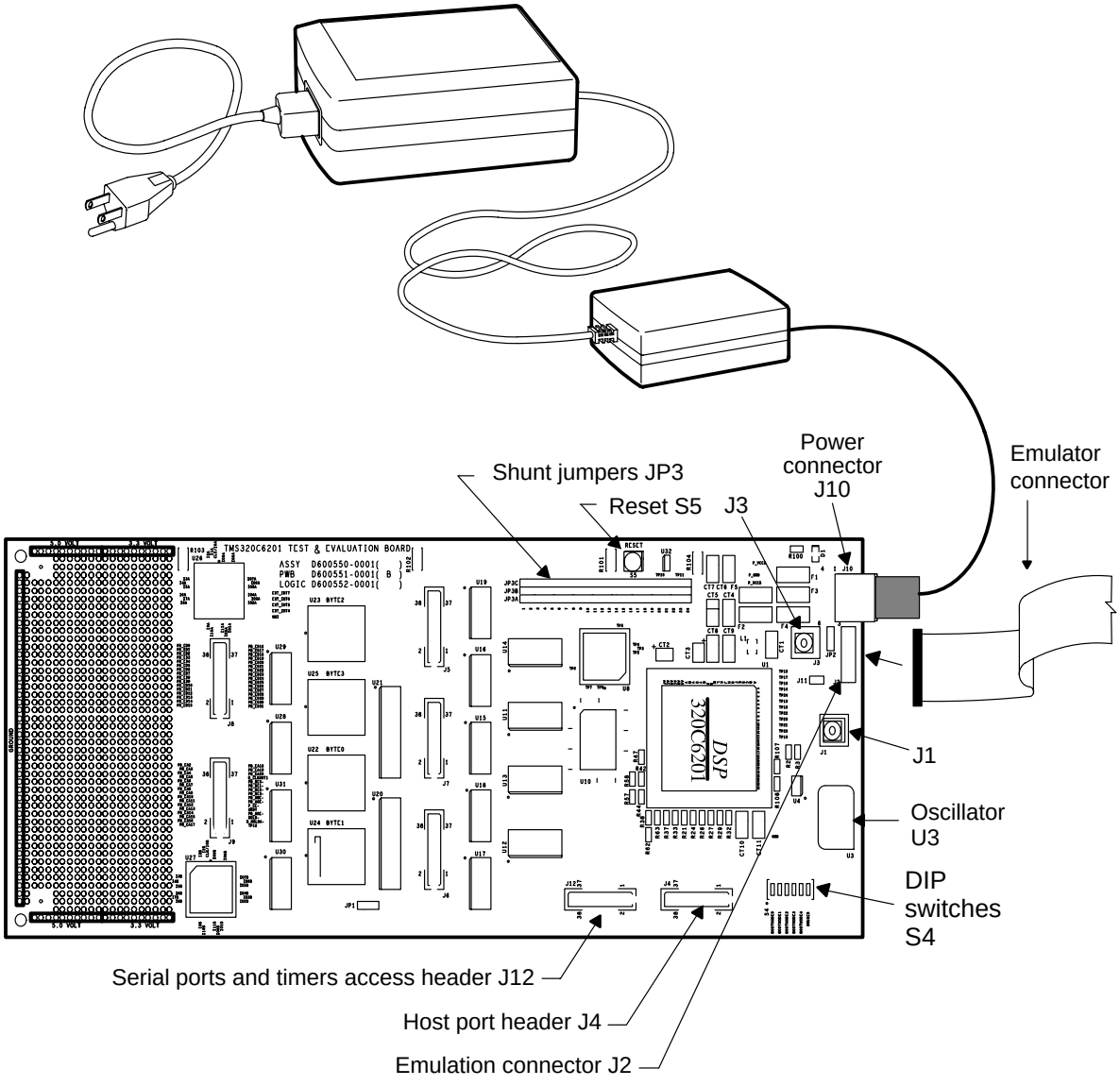
Step 4: Connect the power supply's male 6-pin connector into J10 of the TEB.

Figure 2–3. Connecting the Power Supply to the TEB



Step 5: With moderate downward pressure, connect the 14-pin keyed connector from your emulator to J2 on the TEB.

Figure 2–4. Connecting the Emulator to the TEB



Step 6: Turn on power to the emulator. If you have an XDS510WS emulator controller (for a UNIX workstation), switch on the power. If you have an XDS510 emulator controller (for a PC), turn on your PC.

Step 7: Plug the male end of the power supply's AC line cord into an AC outlet. This applies power to the TEB. An LED on the power supply and one on the TEB indicates that power is applied.

If you need to disconnect the TEB, unplug the TEB, then turn off power to the emulator (using the power switch if you have an XDS510WS or by shutting down Windows and turning off your PC if you have an XDS510).

Chapter 3

TMS320C6201 Test and Evaluation Board Operation

This chapter describes the 'C6201 TEB, its key components, and how they operate. It also provides additional information on the TEB's various interfaces.

The 'C6201 TEB consists of the following components:

- Custom power supply
- TMS320C6201 TEB
  - Memory control
  - Power
  - Reset generation
  - Clock generation
  - Interrupt generation
  - 'C6201 external memory interface
  - 'C6201 host port interface
  - Serial ports and timers interface
  - Emulation interface
  - Prototyping area
  - Shunt jumpers and DIP switches
- 3.5-in floppy diskette

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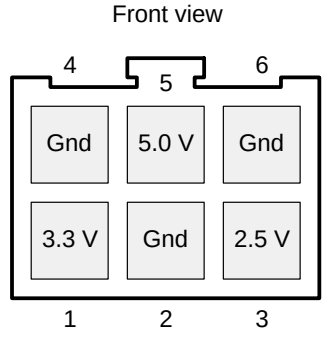
3.1 Custom Power Supply

A custom power supply provides 2.5-, 3.3-, and 5.0-V_{DC} regulated supply voltages to the TEB when connected to an AC wall outlet. An LED on top of the power supply illuminates when it has been properly connected to AC power. The LED blinks when the power supply is connected to a wall outlet where the DC outlet is not connected to the TEB. The TEB's power supply must be loaded to regulate the voltages measured at its DC outlet. Voltages at the DC outlet without the load of the TEB appear unstable.

Figure 3–1. Power Supply DC Connector



3.2 Power Requirements

LED D1 (located next to the power jack on the TEB) illuminates when power is applied to the 6-pin DC power jack J10. See Figure 2–4 for details about applying power to the TEB. Table 3–1 lists the appropriate fuse current ratings to protect the TEB components.

Table 3–1. TEB Fuse Ratings

Voltage	Label	Schematic reference designation	Rating	Purpose of Supply Voltage
2.5	V_{CC2}	F2	7.0 A	'C6201 internals
3.3	V_{CC3}	F1	4.0 A	'C6201 I/Os and TEB 3.3-V components
3.3	P_V_{CC3}	F5	0.75 A	Prototype area 3.3-V components
5.0	V_{CC5}	F3	0.25 A	TEB 5.0-V components
5.0	P_V_{CC5}	F4	1.5 A	Prototype area 5.0-V components

CAUTION

Use only fuses with ratings listed in Table 3–1 to avoid damage to the TEB.

Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.

3.3 Reset Generation

At power up, power down, and during brownout conditions, a supply voltage supervisory circuit forces the ’C6201 DSP into a reset condition. Pressing the push-button switch S5 also forces a reset. In either case, the ’C6201’s reset line is active (low) for a period of at least 200 ms.

3.4 Clock Generation

The ’C6201 DSP operates at frequencies up to 200 MHz. Two options for generation of the clock signal CLKIN are provided on the TEB.

- A 68-Ω resistor installed in location R2 selects oscillator U3.
- Removing R2 and installing it as R3 selects the SMA connector J1 as the source for the CLKIN signal.

These options, combined with the ’C6201’s internal phase-locked loop (PLL), allow you to experiment with different clock frequencies. Use of the PLL in the multiply-by-four mode for a CLKOUT1 frequency other than 133 MHz requires the replacement of components R1, C2, and C3. See the *TMS320C6201 Digital Signal Processor Data Sheet* for more information.

The factory default configuration of the TEB uses a 33.25-MHz oscillator to provide input to the ’C6201’s PLL, which is set to operate in multiply-by-four mode. R2 is installed to select U3 as the source for the ’C6201’s PLL. Shunt jumpers JP3.10 (CLKMODE1) and JP3.9 (CLKMODE0) select the clock multiply-by-four mode. Shunt jumpers JP3.8 (PLLFREQ3)–JP3.6 (PLLFREQ1) select a CLKOUT1 frequency range of 25–135 MHz. The oscillator and the PLL provide a CLKOUT1 signal that has a period of approximately 7.5 ns, a frequency of 133 MHz, and a duty cycle of approximately 50%.

You can operate the ’C6201 internally at frequencies up to 200 MHz by reconfiguring shunt jumpers JP3.10–JP3.6 and replacing the CLKIN source. You must also replace oscillator U3 with a different frequency 5.0-V oscillator. You can use SMA connector J1 by removing and installing the 68 Ω resistor R2 in the location of R3. When changing frequencies, see the *TMS320C6201 Digital Signal Processor Data Sheet* to achieve optimal performance for your desired configuration of the TEB.

3.5 Interrupt Generation

Pressing the push-button switch S5 generates a manual reset of the ’C6201. Shunt jumpers JP3.1 (NMI) and JP3.2 (EXT_INT4)–JP3.5 (EXT_INT7) pull the ’C6201’s external interrupts up or down. The factory default shunt jumper settings must be pulled low because these interrupts are rising-edge sensitive.

Figure 2–1, page 2-3, shows solder connections for the interrupts at the upper right of the prototype area, to the right of U26. You must remove the appropriate interrupt shunt jumper(s) to control these interrupts with non-TEB circuitry (for example, prototype circuitry).

3.6 External Memories

The TEB provides four different types of memory for program execution and data storage. The TEB’s memory types, their speeds and organizations, and the selected ’C6201 chip enable signal are listed in Table 3–2:

Table 3–2. TEB Memories

Memory Type	Designation	Timing (ns)	Organization	Total	’C6201 CE
SBSRAM	U10	6.7	128KB x 32 bits	512KB	CE2
SDRAM	U11–U14	12	2MB x 8 bits	8MB	CE0
ASRAM	U20–U21	12	64KB x 16 bits	256KB	CE3
ROM	U22–U25	200	32KB x 8 bits	128KB	CE1

See the *TMS320C6201 Digital Signal Processor Data Sheet* for a description of the chip enable signals and the processor memory map.

3.7 Host Port Connection

Header J4 connects to the TEB and an off-board (user supplied and programmed) host. The header is an AMP 2–767004–2 and the mating connector part number is AMP 767003–9.

3.8 Serial Ports and Timers Connection

Header J12 allows access to the ’C6201’s serial ports and timers. The header is an AMP 2–767004–2 and the mating connector part number is AMP 767003–9.

Note:

Timer input 0 (TINP0) and timer input 1 (TINP1) are pulled high by the factory default configuration of shunt jumpers JP3.23 and JP3.24, respectively.

3.9 Emulation Port Connection

Emulation connector J2 connects the ’C6201’s emulation port and either the XDS510 or XDS510WS emulator. Shunt jumpers JP3.16 and JP3.17 pull the EMU0 and EMU1 signal up or down. The factory default configuration causes these signals to be pulled up. For more information about emulation signals, see the *JTAG/MPSD Emulation Technical Reference*.

SMA connector J3 allows you to provide an alternative TCK signal. To use the alternative TCK signal, shunt jumper JP2 must be moved from its factory default position to connect pins 1 and 2.

3.10 Prototyping Area

Figure 2–1 shows the through-hole area for prototyping located at the left end of the TEB. This area includes two sockets for user-programmable 3.3-V_{dc} 22V10 PAL® devices (U26 and U27). Fused 3.3-V_{dc} (P_{VCC3}) and 5.0-V_{dc} (P_{VCC5}) supply connections are provided at both the top and bottom edges of the prototyping area. Fuses protect against attempts to draw more current than is allowed by the power supply's design. Ground connections are provided at the extreme left end of the prototyping area.

Connectors J8 and J9 provide connectivity to the 'C6201's external memory interface's data, address, and control busses. These 32-bit connectors provide a direct connection with the modern test equipment cables. (The header part number is AMP 2–767004–2 and the mating connector part number is AMP 767003–9.) All 32 bits of data are available at J8. Only 19 bits of address are available at J9 because the TEB's prototyping area shares the 'C6201's external address space CE1 with the on-board PEROM. Consequently, only asynchronous devices may be interfaced to J8 and J9. PAL® U8 logic equations (Appendix A) control buffers between the asynchronous memory portion of the TEB and the TEB's prototyping area.

The 'C6201's external interrupts are available as test points NMI and EXT_INT4–EXT_INT7. See section 3.5, *Interrupt Generation*, for details about the use of these test points.

Use only fuses with ratings given in Table 3–1 to avoid damage to the TEB.

Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.

3.11 Shunt Jumpers and DIP Switches

You can configure the on-board ’C6201 and TEB devices by changing the settings of shunt jumpers and DIP switches described in Table 3–3 and Table 3–4.

Table 3–3. TEB Shunt Jumpers

Name	Position	Description
ROM protect	JP1	Write protects Flash PEROM 1–2 Writes disabled 2–3 Writes enabled
TCLK select	JP2	Selects JTAG clock 1–2 SMA connector (J3) 2–3 Emulation connector (J2)
NMI	JP3.1	Nonmaskable interrupt A–B Active B–C Inactive NONE Controlled by other logic (prototyping area)
EXT_INT4 EXT_INT5 EXT_INT6 EXT_INT7	JP3.2 JP3.3 JP3.4 JP3.5	External interrupts: edge-driven (rising edge) A–B Active B–C Inactive NONE Controlled by other logic (prototyping area)
PLLFREQ1 PLLFREQ2 PLLFREQ3	JP3.6 JP3.7 JP3.8	Selects one of three frequency ranges for the ’C6201 CLKOUT1 signal

JP3.8	JP3.7	JP3.6	Frequency Range
B–C	B–C	B–C	25–135 MHz
B–C	B–C	A–B	35–160 MHz
B–C	A–B	B–C	40–200 MHz

CLKMODE0 CLKMODE1	JP3.9 JP3.10	Clock mode select. Selects the multiplication factor of the input clock frequency. CLKOUT1 is 1x or 4x CLKIN:

JP3.10	JP3.9	Clock Mode
B–C	B–C	PLL multiply-by-one mode
B–C	A–B	Reserved
A–B	B–C	Reserved
A–B	A–B	PLL multiply-by-four mode

Table 3–3. TEB Shunt Jumpers (Continued)

Name	Position	Description
RSV0	JP3.11	Reserved
RSV1	JP3.12	
RSV2	JP3.13	
RSV3	JP3.14	
RSV4	JP3.15	
EMU0	JP3.16	TI emulation support
EMU1	JP3.17	
LENDIAN	JP3.18	Selects endianess of addressing B–C Big endian A–B Little endian
ARDY	JP3.19	Asynchronous memory ready signal
HOLD–	JP3.20	Hold request from host (external memory interface bus arbitration)
UNUSED	JP3.21	Unused
UNUSED	JP3.22	Unused
TINP0	JP3.23	Timer input 0
TINP1	JP3.24	Timer input 1

Note: A–B indicates HIGH (1)
B–C indicates LOW (0)

Table 3–4. TEB DIP Switches

Name	Position	Description
BOOTMODE0	S4.1	Boot mode configuration. See the *TMS320C62xx Peripherals Reference Guide* for a complete description.
BOOTMODE1	S4.2	
BOOTMODE2	S4.3	
BOOTMODE3	S4.4	
BOOTMODE4	S4.5	
SWUSER	S4.6	User-defined input to U8 PAL®

Appendix A

TMS320C6201 TEB PAL® Equations

This appendix contains the programmable logic source for the TMS320C6201 test and evaluation board PAL® equations. These were compiled with DATA I/O ABEL™ version 4.0.

```
module U8_MLA
Title '
PAL NAME    Memory Logic Block A (PAL MLA)
PAL #       U8, D600555–1741*
DWG NAME    TMS320C6201 Test & Evaluation Board
ASSY #      D600550–0001B
COMPANY     Texas Instruments, Incorporated

SYNTHESIS TOOL: ABEL–4 Design Environment v1.0'

  U8 device 'P22V10C'; "The PALLV22V10 is a 28–pin PLCC

  "NC             pin  1; NO CONNECT
  clkout1         pin  2; "Clock out 1 from C6201
  ce1_            pin  3; "Chip enable 1 from C6201
  awe_            pin  4; "Asynchronous write enable from C6201
  aoe_            pin  5; "Asynchronous output enable from C6201
  ea21            pin  6; "EMIF address bit 21 from C6201
  ce3_            pin  7; "Chip enable 3 from C6201
  "NC             pin  8; NO CONNECT
  tp2             pin  9; "Test point(2) input – undefined
  tp3             pin 10; "Test point(3) input – undefined
  tp4             pin 11; "Test point(4) input – undefined
  tp5             pin 12; "Test point(5) input – undefined
  swuser          pin 13; "Switch input – user defined
  GND             pin 14; "Ground
  "NC             pin 15; NO CONNECT
  reset_          pin 16; "Reset
  a_dir           pin 17; "Asynchronous direction
  a_oe_           pin 18; "Asynchronous buffer output enable
  romce_          pin 19; "ROM Chip Enable
  p_ce_           pin 20; "Prototype chip enable
  p_dir           pin 21; "Prototype buffer direction
  "NC             pin 22; NO CONNECT
  p_dboe_         pin 23; "Prototype data buffer output enable
  p_aboe_         pin 24; "Prototype addr buffer output enable
  tp6             pin 25; "Test point(6) output – undefined
  tp7             pin 26; "Test point(7) output – undefined
  tp8             pin 27; "Test point(8) output – undefined
  VCC             pin 28; "Power
```

```
Equations

 "Because the TMS320C6201 may be in part of a write cycle (i.e., setup or hold
 "time) when awe_ is inactive, the aoe_ signal should be used to determine the
 "direction of the access.

"axoez  axwez  Access
"-----  -----  ------------------------------------------------------------
"  0      0    Invalid combination with the DSP
"               Should not happen so disable the buffers

"  0      1    Read from asynchronous type to the DSP
"               Should cause buffers to output towards the DSP

"  1      0    Write (strobe) to asynchronous type from the DSP
"               Should cause buffers to output towards async type

"  1      1    Could be part of a write cycle (i.e., write setup or hold time)
"               Should cause buffers to output towards async type

 a_dir   = aoe_;              "A->B (i.e., DSP to external memories) when 1,
                              "B->A (i.e., external memories to DSP) when 0
 a_oe_   = (ce1_ & ce3_ & awe_ & aoe_) # (!awe_ & !aoe_);



 romce_  = ce1_ # ea21;          "Select flash ROM when ea21 = 0
 p_ce_   = ce1_ # !ea21;         "Select Prototype area when ea21 = 1
 p_dir   = !(!ce1_ & ea21) # aoe_;
 p_dboe_ = (awe_ & aoe_) # (!awe_ & !aoe_) # ce1_ # !ea21;
 p_aboe_ = 0;


Test_Vectors
 ([ ce1_, ce3_,aoe_, awe_] -> [a_dir, a_oe_])
  [  1  ,  1  , 0  ,  0  ] -> [  0  ,   1  ];
  [  1  ,  1  , 0  ,  1  ] -> [  0  ,   0  ];
  [  1  ,  1  , 1  ,  0  ] -> [  1  ,   0  ];
  [  1  ,  0  , 1  ,  1  ] -> [  1  ,   0  ];
  [  0  ,  1  , 1  ,  1  ] -> [  1  ,   0  ];
  [  1  ,  1  , 1  ,  1  ] -> [  1  ,   1  ];
```

```
Test_Vectors
 ([ce1_, ea21, aoe_, awe_] -> [romce_, p_ce_, p_dir, p_dboe_, p_aboe_])
  [ 0  ,  0  ,  0  ,  0  ] -> [  0   ,   1  ,   1  ,    1   ,    0   ];
  [ 0  ,  0  ,  0  ,  1  ] -> [  0   ,   1  ,   1  ,    1   ,    0   ];
  [ 0  ,  0  ,  1  ,  0  ] -> [  0   ,   1  ,   1  ,    1   ,    0   ];
  [ 0  ,  0  ,  1  ,  1  ] -> [  0   ,   1  ,   1  ,    1   ,    0   ];
  [ 0  ,  1  ,  0  ,  0  ] -> [  1   ,   0  ,   0  ,    1   ,    0   ];
  [ 0  ,  1  ,  0  ,  1  ] -> [  1   ,   0  ,   0  ,    0   ,    0   ];
  [ 0  ,  1  ,  1  ,  0  ] -> [  1   ,   0  ,   1  ,    0   ,    0   ];
  [ 0  ,  1  ,  1  ,  1  ] -> [  1   ,   0  ,   1  ,    1   ,    0   ];

  [ 1  ,  0  ,  0  ,  0  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  0  ,  0  ,  1  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  0  ,  1  ,  0  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  0  ,  1  ,  1  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  1  ,  0  ,  0  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  1  ,  0  ,  1  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  1  ,  1  ,  0  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];
  [ 1  ,  1  ,  1  ,  1  ] -> [  1   ,   1  ,   1  ,    1   ,    0   ];


end
```

Appendix B

TMS320C6201 TEB Schematics

This appendix contains the schematics for the TMS320C6201 TEB.

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS.

2. CAPACITANCE VALUES ARE IN MICROFARADS.

3. HIGHEST REFERENCE DESIGNATOR USED:
   - A. CERAMIC CAPS C71
   - B. TANTALUM CAPS CT11
   - C. DIODES D1
   - D. FUSES F5
   - E. CONNECTORS/HEADERS J12
   - F. SHUNTS JP3
   - G. FILTER L1
   - H. RESISTORS R108
   - I. SWITCHES S5
   - J. TEST POINTS TP24
   - K. IC'S U32

4. UNUSED REFERENCE DESIGNATORS:
   - A. RESISTORS R4,R97
   - B. SWITCHES S1,S2,S3
   - C. TEST POINTS TP1
   - D. IC'S U2,U5,U6,U7,U9

5. U1A–U1I COMPRISE A SINGLE TMS320C6201. THIS IS A 352–CONTACT BGA DEVICE THAT IS TOO LARGE TO SHOW ON A SINGLE SHEET. THIS REVISION OF THE BOARD IS COMPATIBLE WITH REV 2.X OF THE C6201 SILICON

6. ALL FOUR SHIELD CONNECTIONS OF J1 AND J3 MUST CONNECT TO THE GROUND PLANE.

7. SHUNTS FOR NMI AND EXT_INT4–EXT_INT7, AS APPROPRIATE, MUST NOT BE PULLED UP(VCC3) OR DOWN(GND) FOR CONTROL OF THESE SIGNALS.

8. PAGE ORDER AND NUMBERING MAY CHANGE BETWEEN REVISIONS OF THE SCHEMATICS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECN970401(E) M. DAWKINS 4–3–97	6–6–97	J. CLARK
	FORMAL RELEASE		
B	ECN10289(B) M. DAWKINS 9–8–97	9–11–97	J. CLARK
C	ECNxxxxx(E) M. DAWKINS		

REVISION STATUS OF SHEETS

REV	C	C	C	C	C	C	C		
SH	15	16	17	18	19	20	21		
REV	C	C	C	C	C	C	C		
SH	8	9	10	11	12	13	14	D600550	
REV	C	C	C	C	C	C	C	NEXT ASSY	USED ON
SH	1	2	3	4	5	6	7	APPLICATION	

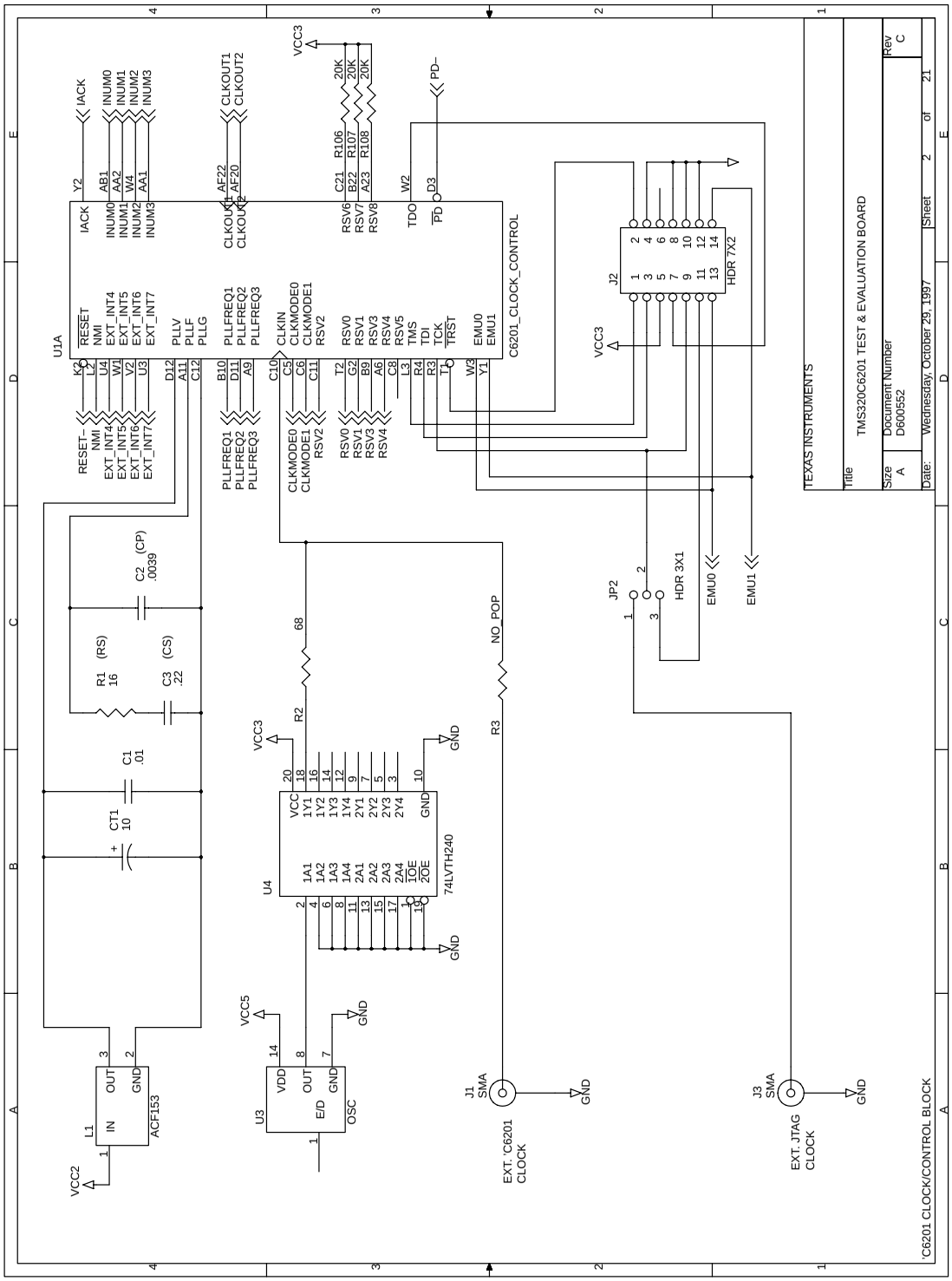
DWN	G. CONNELLY	DATE 1–20–97
CHK	M. DAVIS	DATE 6–6–97
ENGR	G. CONNELLY	DATE 6–6–97
ENGR–MGR	R. LERNER	DATE 6–6–97
QA	J. WHISONANT	DATE 6–6–97
MFG	M. JACKSON	DATE 6–6–97
RLSE	J. CLARK	DATE 6–6–97

TEXAS INSTRUMENTS
SOFTWARE DEVELOPMENT SYSTEMS
SEMICONDUCTOR GROUP
HOUSTON, TEXAS

Title: TMS320C6201 TEST & EVALUATION BOARD

Size	Document Number	Rev
A	D600552	C

Date: Wednesday, October 29, 1997 Sheet 1 of 21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Rev C
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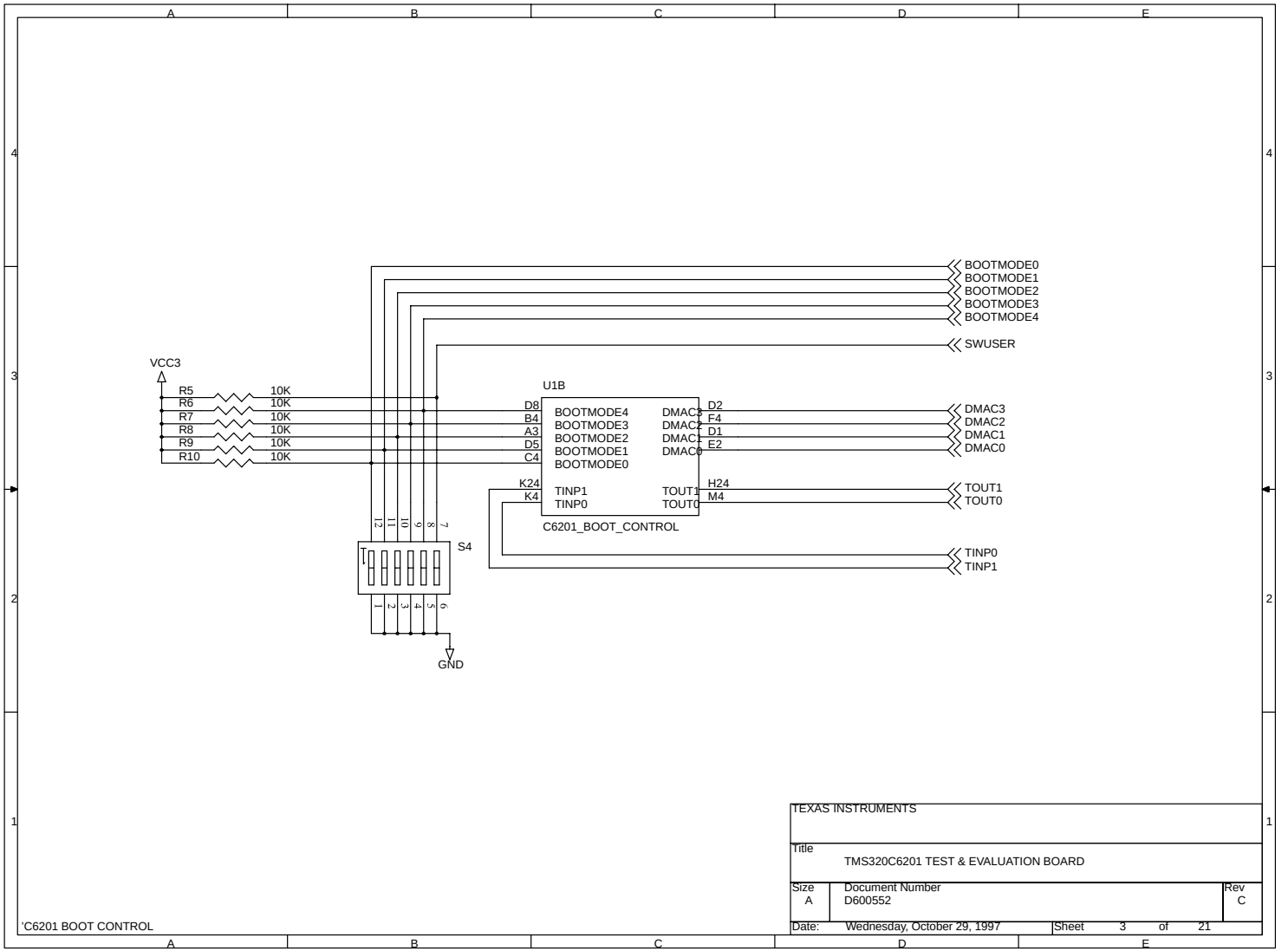
IACK
INUM0
INUM1
INUM2
INUM3
CLKOUT1
CLKOUT2
PD
RESET
NMI
EXT_INT4
EXT_INT5
EXT_INT6
EXT_INT7
PLLV
PLLF
PLLG
PLLFREQ1
PLLFREQ2
PLLFREQ3
CLKIN
CLKMODE0
CLKMODE1
RSV2
RSV0
RSV1
RSV3
RSV4
RSV5
TMS
TDI
TCK
TRST
EMU0
EMU1
TDO
RSV6
RSV7
RSV8
20K
R106
R107
R108
HDR 7X2
J2
HDR 3X1
JP2
EMU0
EMU1
NO_POP
R1 16 (RS)
C2 .0039 (CP)
C3 .22 (CS)
C1 .01
CT1 10
R2 68
R3
U4 74LVTH240
U3 OSC
VCC2
VCC3
VCC5
GND
L1 ACF153
J1 SMA
EXT. 'C6201 CLOCK
J3 SMA
EXT. JTAG CLOCK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B
C
D
E
4
3
2
1
BOOTMODE0
BOOTMODE1
BOOTMODE2
BOOTMODE3
BOOTMODE4
SWUSER
VCC3
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R10 10K
U1B
D8 BOOTMODE4
B4 BOOTMODE3
A3 BOOTMODE2
D5 BOOTMODE1
C4 BOOTMODE0
K24 TINP1
K4 TINP0
DMAC3 D2
DMAC2 F4
DMAC1 D1
DMAC0 E2
TOUT1 H24
TOUT0 M4
C6201_BOOT_CONTROL
DMAC3
DMAC2
DMAC1
DMAC0
TOUT1
TOUT0
TINP0
TINP1
S4
GND
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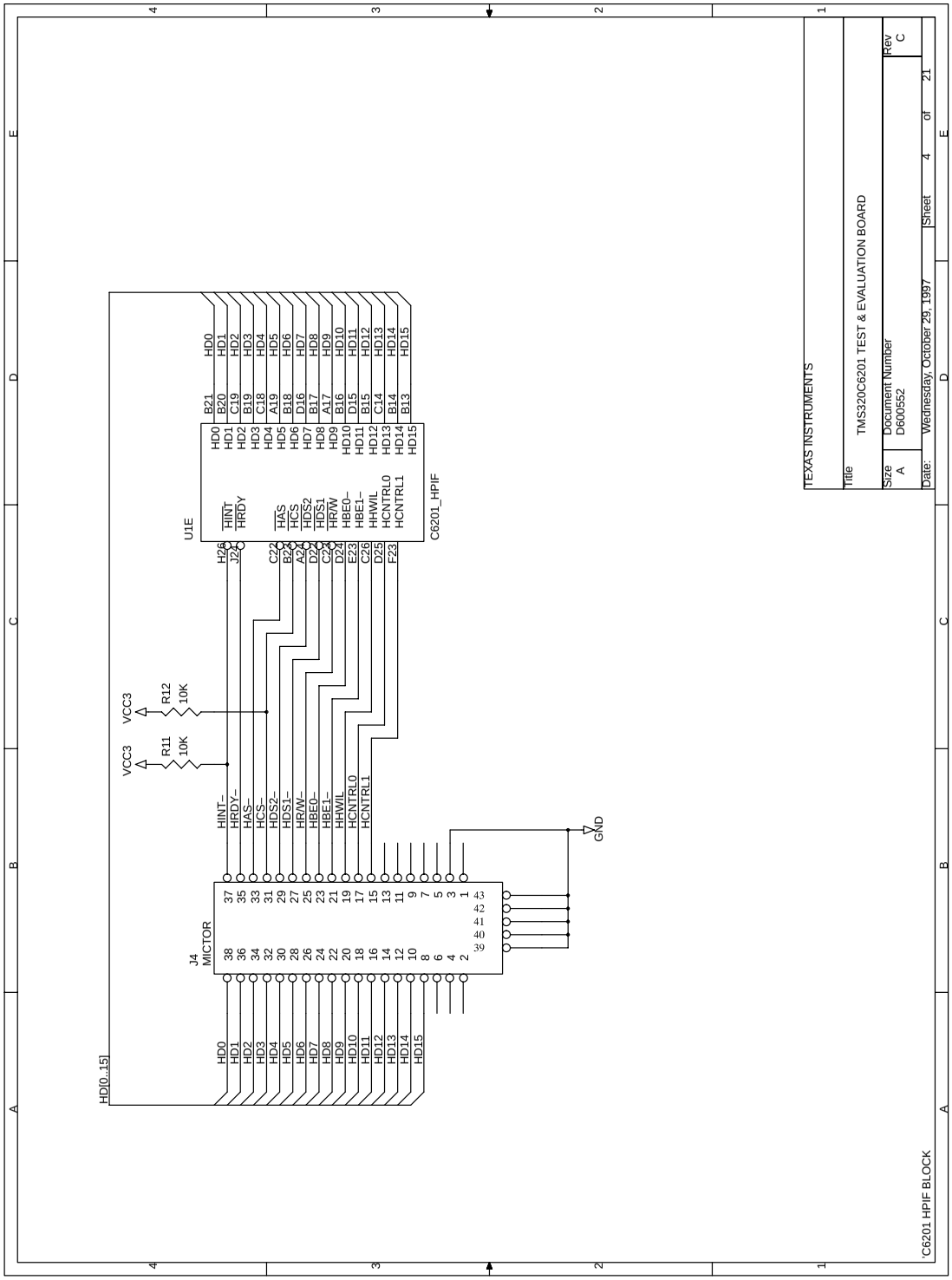
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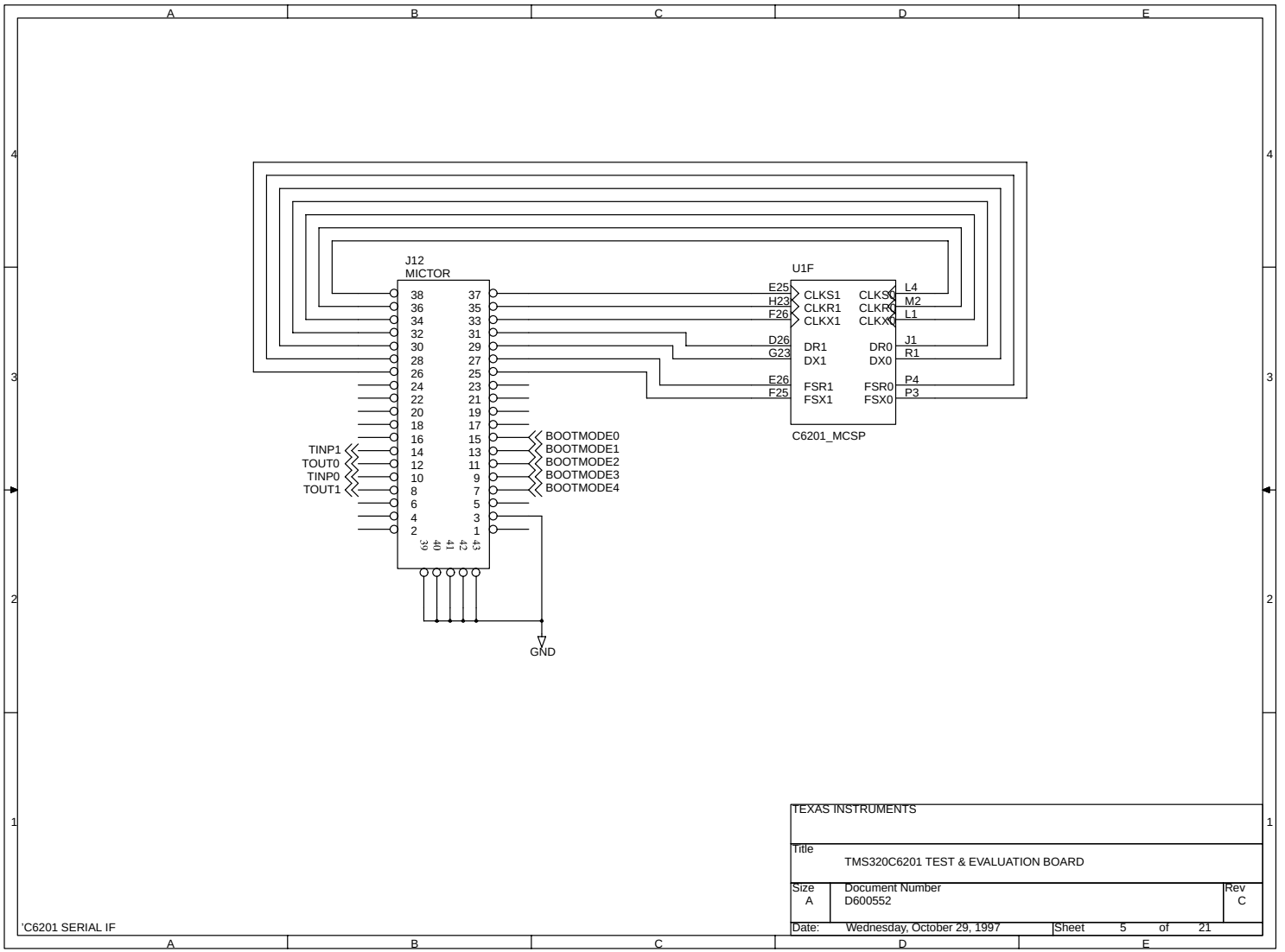
C6201_HPIF
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
HD8
HD9
HD10
HD11
HD12
HD13
HD14
HD15
HINT
HRDY
HAS
HCS
HDS2
HDS1
HR/W
HBE0–
HBE1–
HHWIL
HCNTRL0
HCNTRL1
HD[0..15]
J4
MICTOR
VCC3
R12
10K
R11
10K
GND


A
B
C
D
E
4
3
2
1
J12
MICTOR
38 37
36 35
34 33
32 31
30 29
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26 25
24 23
22 21
20 19
18 17
16 15
14 13
12 11
10 9
8 7
6 5
4 3
2 1
39 40 41 42 43
TINP1
TOUT0
TINP0
TOUT1
BOOTMODE0
BOOTMODE1
BOOTMODE2
BOOTMODE3
BOOTMODE4
GND
U1F
E25 CLKS1 CLKS0 L4
H23 CLKR1 CLKR0 M2
F26 CLKX1 CLKX0 L1
D26 DR1 DR0 J1
G23 DX1 DX0 R1
E26 FSR1 FSR0 P4
F25 FSX1 FSX0 P3
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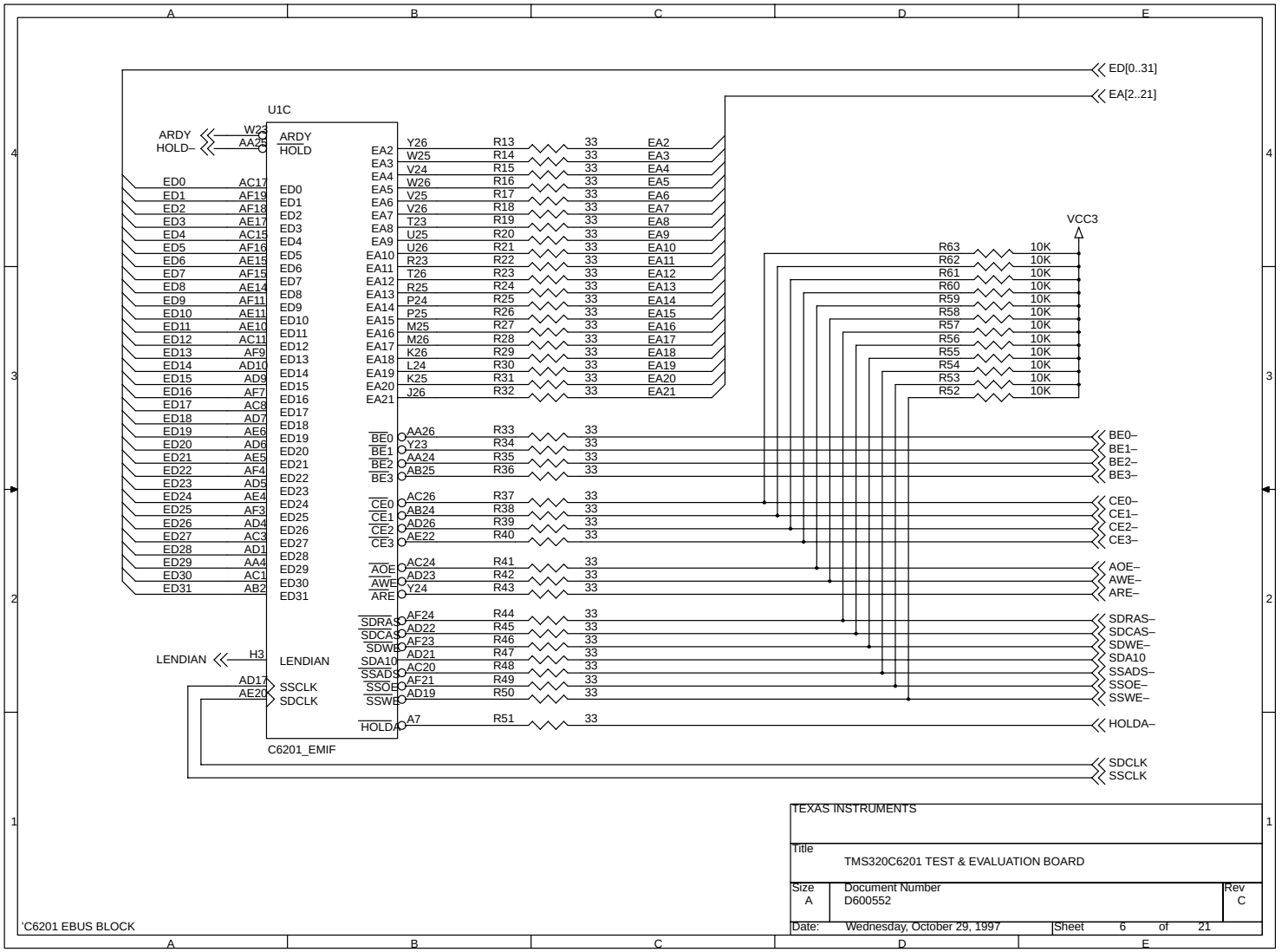
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HOLD–
LENDIAN
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SDCLK
C6201_EMIF
VCC3
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R62 10K
R61 10K
R60 10K
R59 10K
R58 10K
R57 10K
R56 10K
R55 10K
R54 10K
R53 10K
R52 10K
BE0–
BE1–
BE2–
BE3–
CE0–
CE1–
CE2–
CE3–
AOE–
AWE–
ARE–
SDRAS–
SDCAS–
SDWE–
SDA10
SSADS–
SSOE–
SSWE–
HOLDA–
SDCLK
SSCLK
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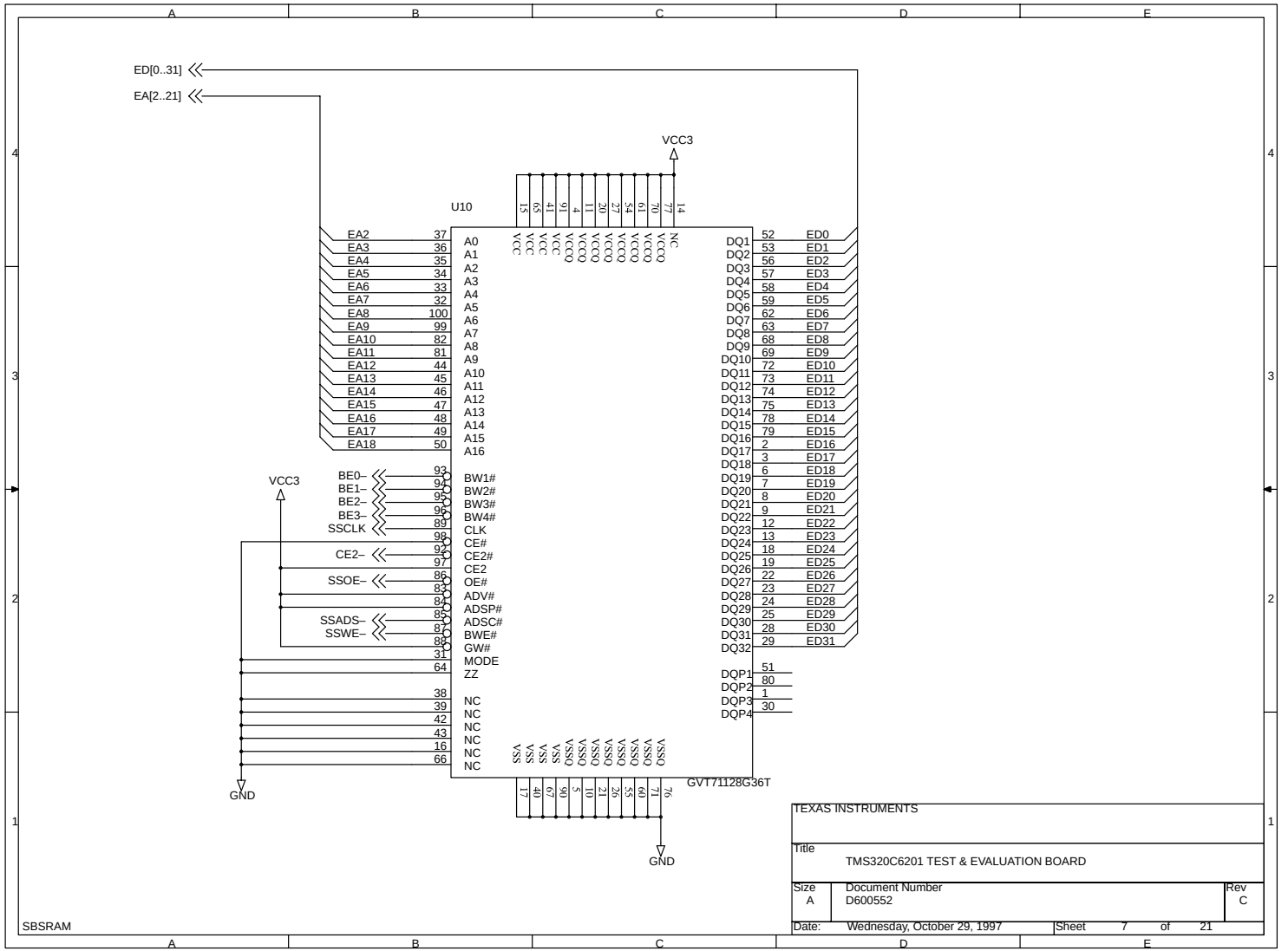
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EA[2..21]
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U10
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EA3 36 A1
EA4 35 A2
EA5 34 A3
EA6 33 A4
EA7 32 A5
EA8 100 A6
EA9 99 A7
EA10 82 A8
EA11 81 A9
EA12 44 A10
EA13 45 A11
EA14 46 A12
EA15 47 A13
EA16 48 A14
EA17 49 A15
EA18 50 A16
BE0– 93 BW1#
BE1– 94 BW2#
BE2– 95 BW3#
BE3– 96 BW4#
SSCLK 89 CLK
98 CE#
CE2– 92 CE2#
97 CE2
SSOE– 86 OE#
83 ADV#
84 ADSP#
SSADS– 85 ADSC#
SSWE– 87 BWE#
88 GW#
31 MODE
64 ZZ
38 NC
39 NC
42 NC
43 NC
16 NC
66 NC
DQ1 52 ED0
DQ2 53 ED1
DQ3 56 ED2
DQ4 57 ED3
DQ5 58 ED4
DQ6 59 ED5
DQ7 62 ED6
DQ8 63 ED7
DQ9 68 ED8
DQ10 69 ED9
DQ11 72 ED10
DQ12 73 ED11
DQ13 74 ED12
DQ14 75 ED13
DQ15 78 ED14
DQ16 79 ED15
DQ17 2 ED16
DQ18 3 ED17
DQ19 6 ED18
DQ20 7 ED19
DQ21 8 ED20
DQ22 9 ED21
DQ23 12 ED22
DQ24 13 ED23
DQ25 18 ED24
DQ26 19 ED25
DQ27 22 ED26
DQ28 23 ED27
DQ29 24 ED28
DQ30 25 ED29
DQ31 28 ED30
DQ32 29 ED31
DQP1 51
DQP2 80
DQP3 1
DQP4 30
VCC 15
VCC 65
VCC 41
VCC 91
VCCQ 4
VCCQ 11
VCCQ 20
VCCQ 27
VCCQ 54
VCCQ 61
VCCQ 70
VCCQ 77
NC 14
VSS 17
VSS 40
VSS 67
VSS 90
VSSQ 5
VSSQ 10
VSSQ 21
VSSQ 26
VSSQ 55
VSSQ 60
VSSQ 71
VSSQ 76
GVT71128G36T
GND
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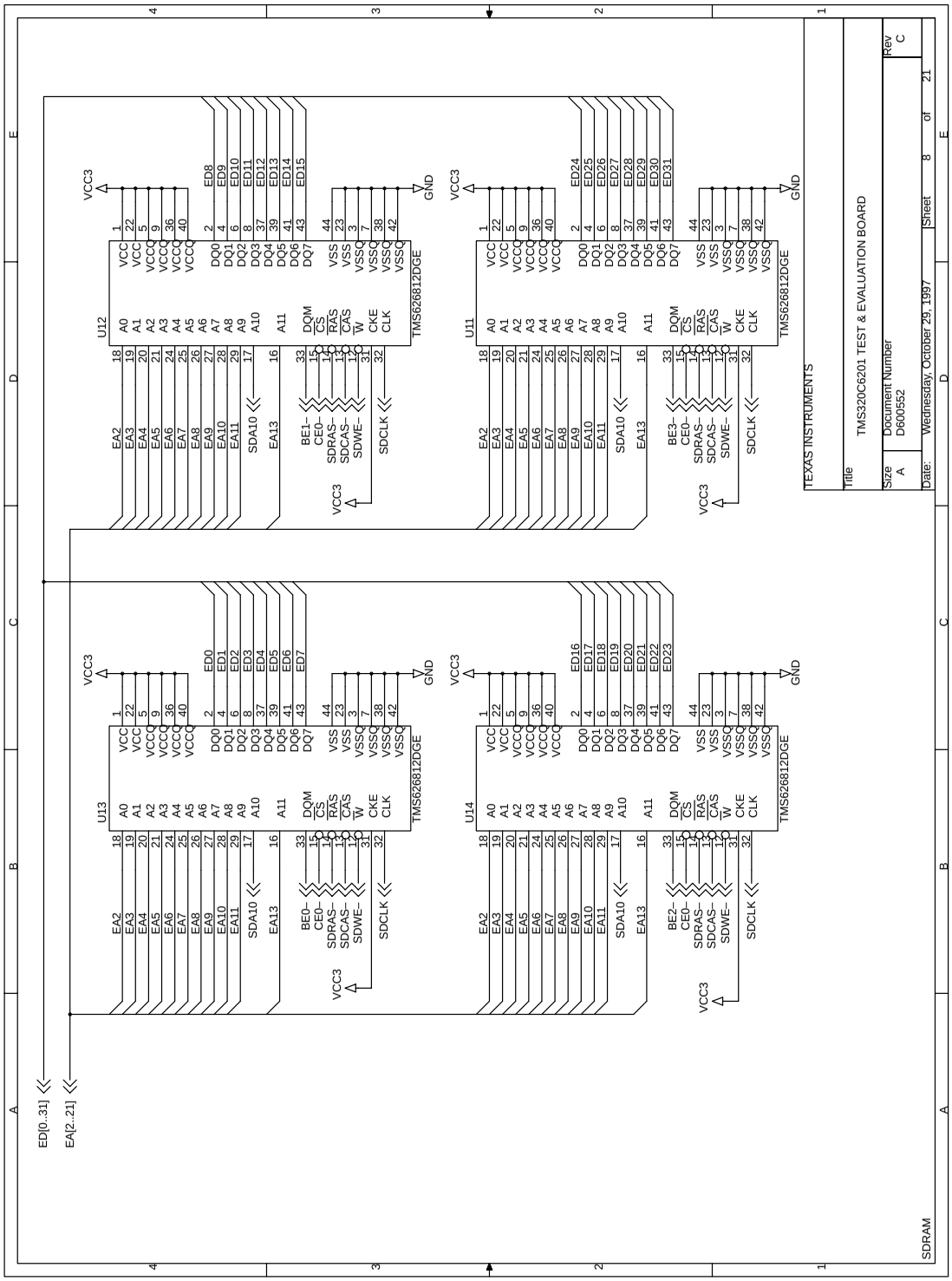
SBSRAM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A
Document Number
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Date: Wednesday, October 29, 1997
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ED[0..31]
EA[2..21]
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U12
U13
U14
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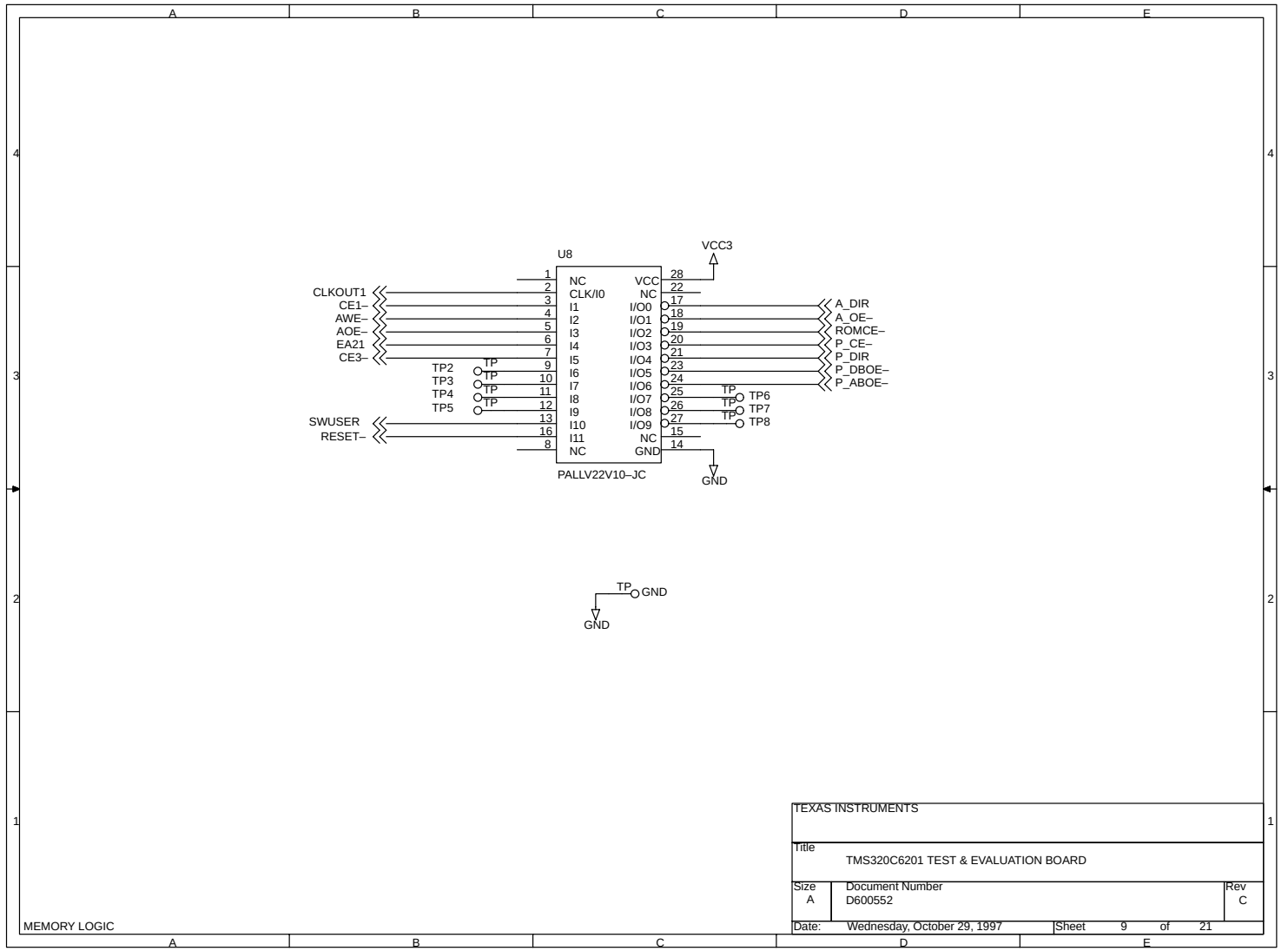
VCC3
GND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B
C
D
E
1
2
3
4
U8
VCC3
NC
CLK/I0
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
NC
VCC
NC
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
I/O9
NC
GND
PALLV22V10–JC
GND
CLKOUT1
CE1–
AWE–
AOE–
EA21
CE3–
SWUSER
RESET–
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP
GND
A_DIR
A_OE–
ROMCE–
P_CE–
P_DIR
P_DBOE–
P_ABOE–
MEMORY LOGIC
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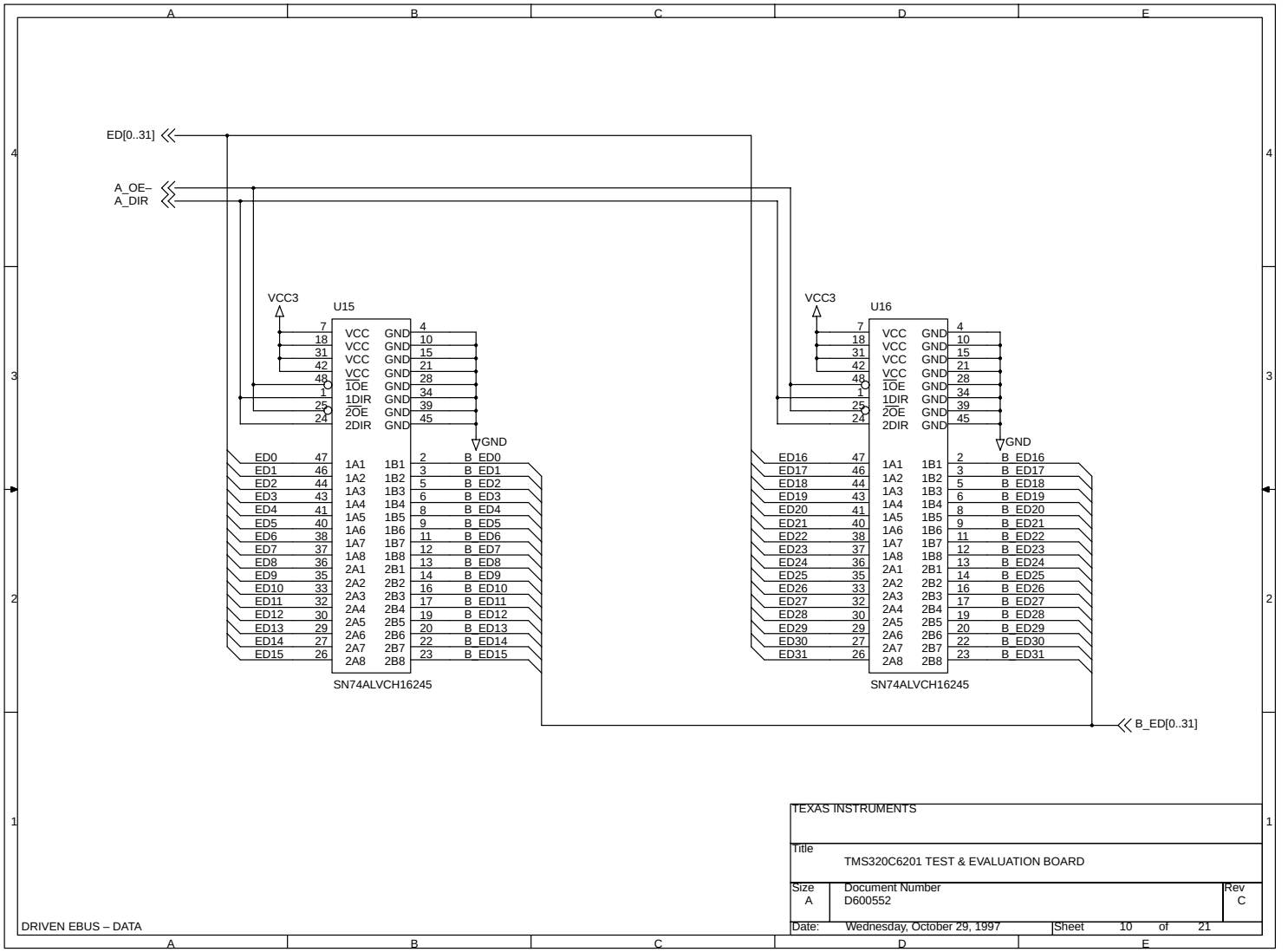
ED[0..31]
A_OE–
A_DIR
VCC3
U15
U16
GND
SN74ALVCH16245
B_ED[0..31]
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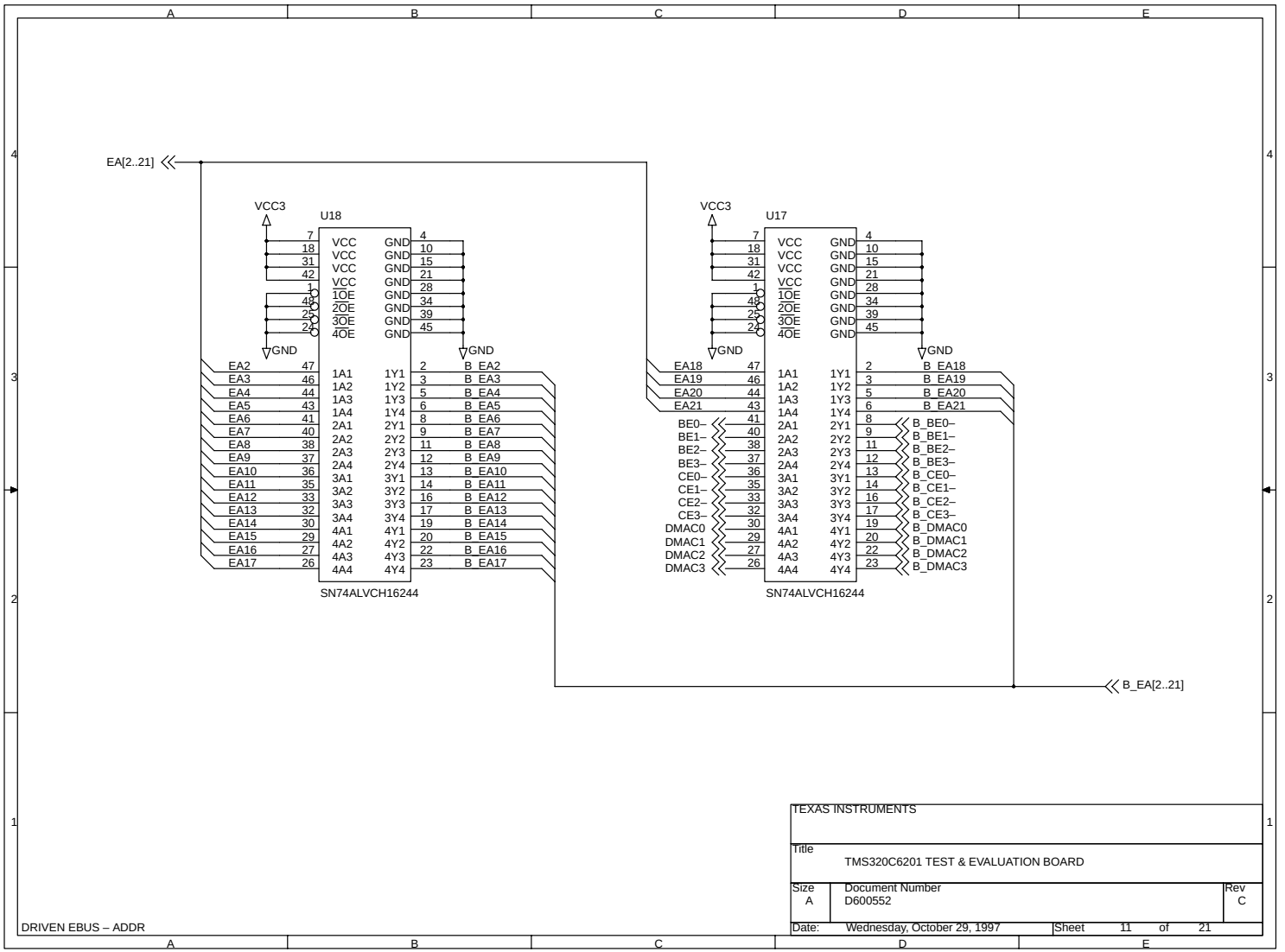
DRIVEN EBUS – DATA


EA[2..21]
VCC3
U18
VCC
GND
1OE
2OE
3OE
4OE
EA2
EA3
EA4
EA5
EA6
EA7
EA8
EA9
EA10
EA11
EA12
EA13
EA14
EA15
EA16
EA17
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
3A1
3A2
3A3
3A4
4A1
4A2
4A3
4A4
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
3Y1
3Y2
3Y3
3Y4
4Y1
4Y2
4Y3
4Y4
B_EA2
B_EA3
B_EA4
B_EA5
B_EA6
B_EA7
B_EA8
B_EA9
B_EA10
B_EA11
B_EA12
B_EA13
B_EA14
B_EA15
B_EA16
B_EA17
SN74ALVCH16244
U17
EA18
EA19
EA20
EA21
BE0–
BE1–
BE2–
BE3–
CE0–
CE1–
CE2–
CE3–
DMAC0
DMAC1
DMAC2
DMAC3
B_EA18
B_EA19
B_EA20
B_EA21
B_BE0–
B_BE1–
B_BE2–
B_BE3–
B_CE0–
B_CE1–
B_CE2–
B_CE3–
B_DMAC0
B_DMAC1
B_DMAC2
B_DMAC3
B_EA[2..21]
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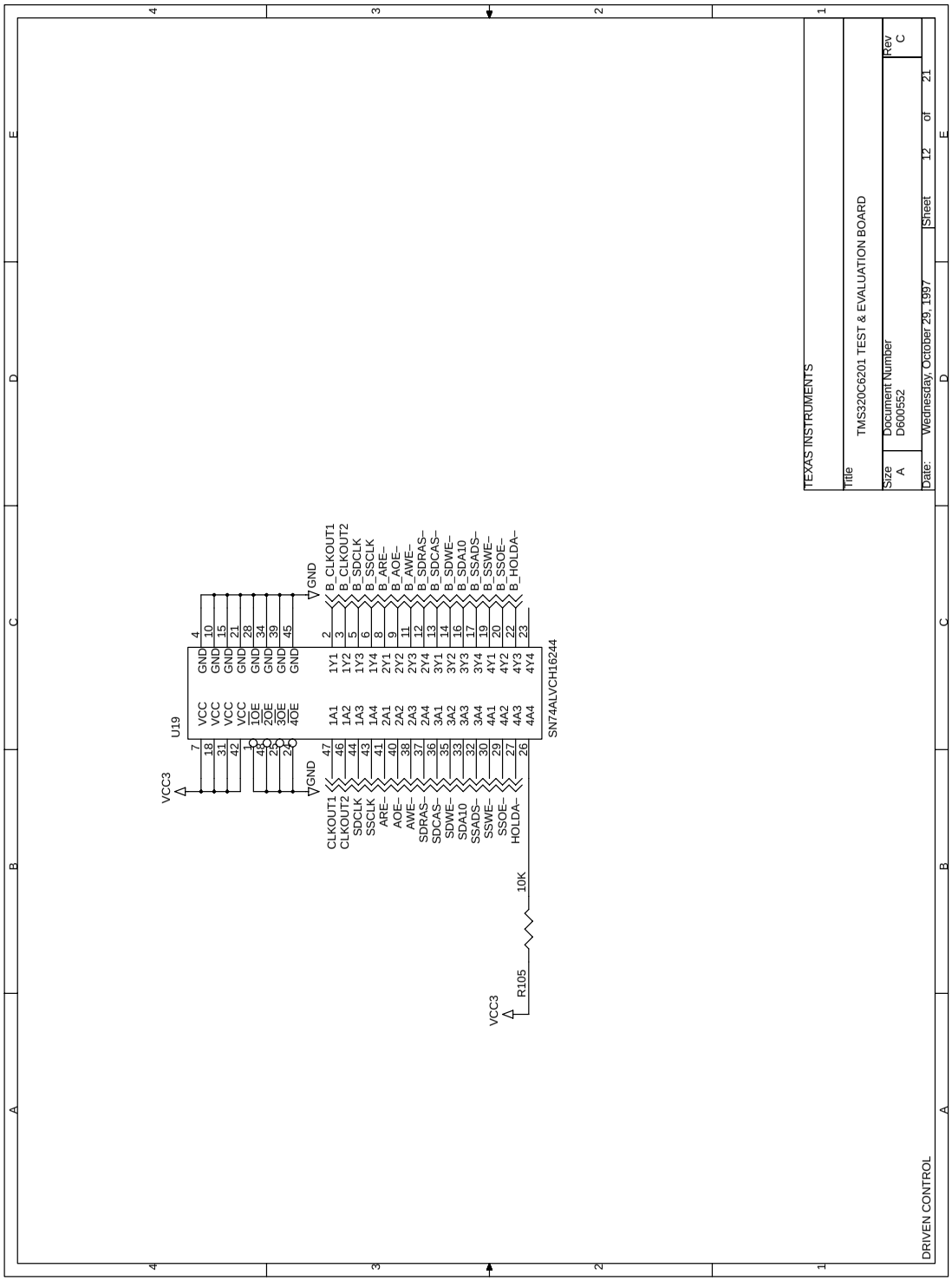
DRIVEN EBUS – ADDR


DRIVEN CONTROL
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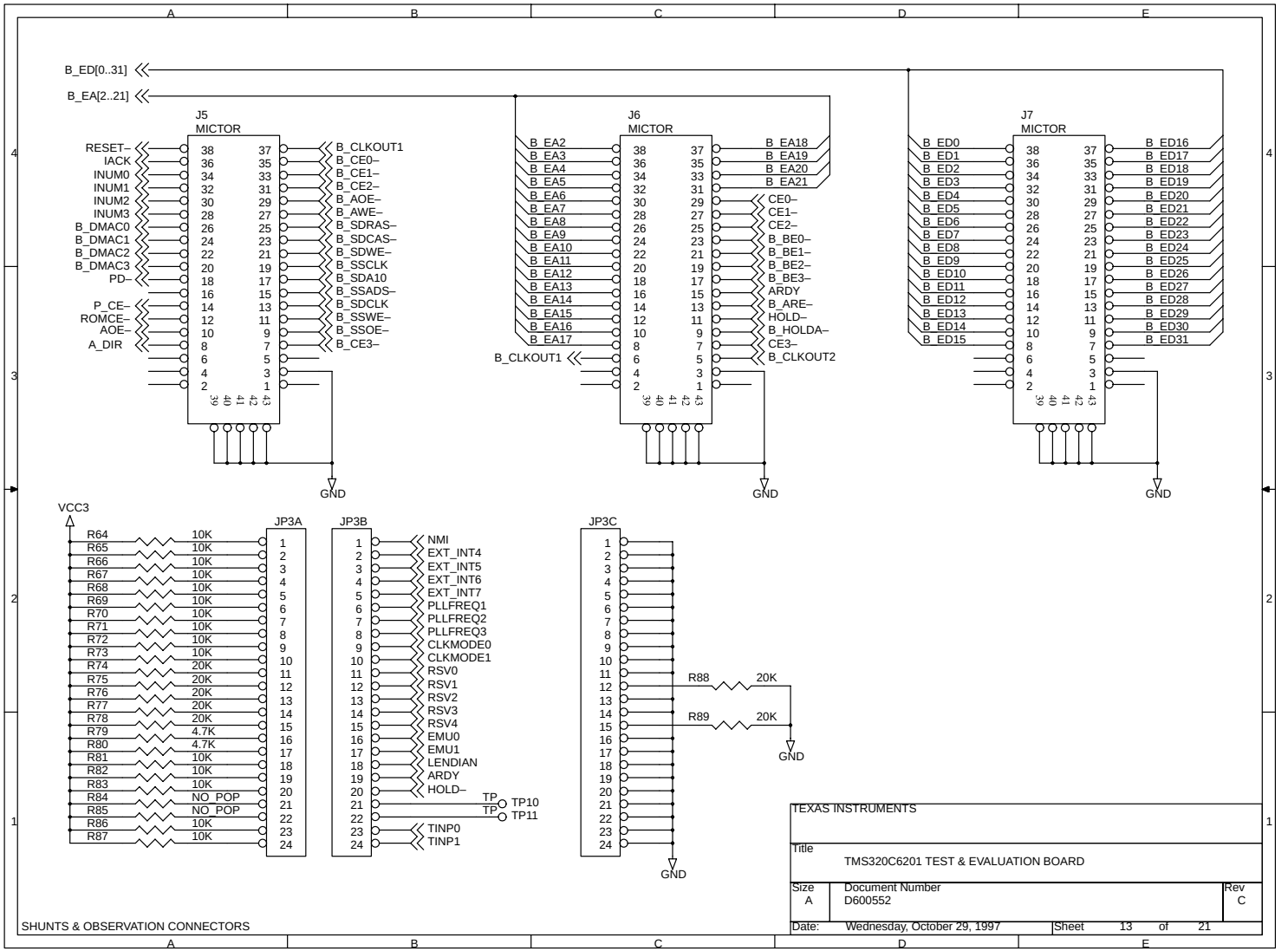
U19
SN74ALVCH16244
VCC3
GND
R105
10K
B_CLKOUT1
B_CLKOUT2
B_SDCLK
B_SSCLK
B_ARE–
B_AOE–
B_AWE–
B_SDRAS–
B_SDCAS–
B_SDWE–
B_SDA10
B_SSADS–
B_SSWE–
B_SSOE–
B_HOLDA–
CLKOUT1
CLKOUT2
SDCLK
SSCLK
ARE–
AOE–
AWE–
SDRAS–
SDCAS–
SDWE–
SDA10
SSADS–
SSWE–
SSOE–
HOLDA–


B_ED[0..31]
B_EA[2..21]
J5
MICTOR
RESET–
IACK
INUM0
INUM1
INUM2
INUM3
B_DMAC0
B_DMAC1
B_DMAC2
B_DMAC3
PD–
P_CE–
ROMCE–
AOE–
A_DIR
B_CLKOUT1
B_CE0–
B_CE1–
B_CE2–
B_AOE–
B_AWE–
B_SDRAS–
B_SDCAS–
B_SDWE–
B_SSCLK
B_SDA10
B_SSADS–
B_SDCLK
B_SSWE–
B_SSOE–
B_CE3–
GND
J6
MICTOR
B_EA2
B_EA3
B_EA4
B_EA5
B_EA6
B_EA7
B_EA8
B_EA9
B_EA10
B_EA11
B_EA12
B_EA13
B_EA14
B_EA15
B_EA16
B_EA17
B_CLKOUT1
B_EA18
B_EA19
B_EA20
B_EA21
CE0–
CE1–
CE2–
B_BE0–
B_BE1–
B_BE2–
B_BE3–
ARDY
B_ARE–
HOLD–
B_HOLDA–
CE3–
B_CLKOUT2
GND
J7
MICTOR
B_ED0
B_ED1
B_ED2
B_ED3
B_ED4
B_ED5
B_ED6
B_ED7
B_ED8
B_ED9
B_ED10
B_ED11
B_ED12
B_ED13
B_ED14
B_ED15
B_ED16
B_ED17
B_ED18
B_ED19
B_ED20
B_ED21
B_ED22
B_ED23
B_ED24
B_ED25
B_ED26
B_ED27
B_ED28
B_ED29
B_ED30
B_ED31
GND
VCC3
R64 10K
R65 10K
R66 10K
R67 10K
R68 10K
R69 10K
R70 10K
R71 10K
R72 10K
R73 10K
R74 20K
R75 20K
R76 20K
R77 20K
R78 20K
R79 4.7K
R80 4.7K
R81 10K
R82 10K
R83 10K
R84 NO_POP
R85 NO_POP
R86 10K
R87 10K
JP3A
JP3B
NMI
EXT_INT4
EXT_INT5
EXT_INT6
EXT_INT7
PLLFREQ1
PLLFREQ2
PLLFREQ3
CLKMODE0
CLKMODE1
RSV0
RSV1
RSV2
RSV3
RSV4
EMU0
EMU1
LENDIAN
ARDY
HOLD–
TP
TP10
TP
TP11
TINP0
TINP1
JP3C
R88 20K
R89 20K
GND
SHUNTS & OBSERVATION CONNECTORS
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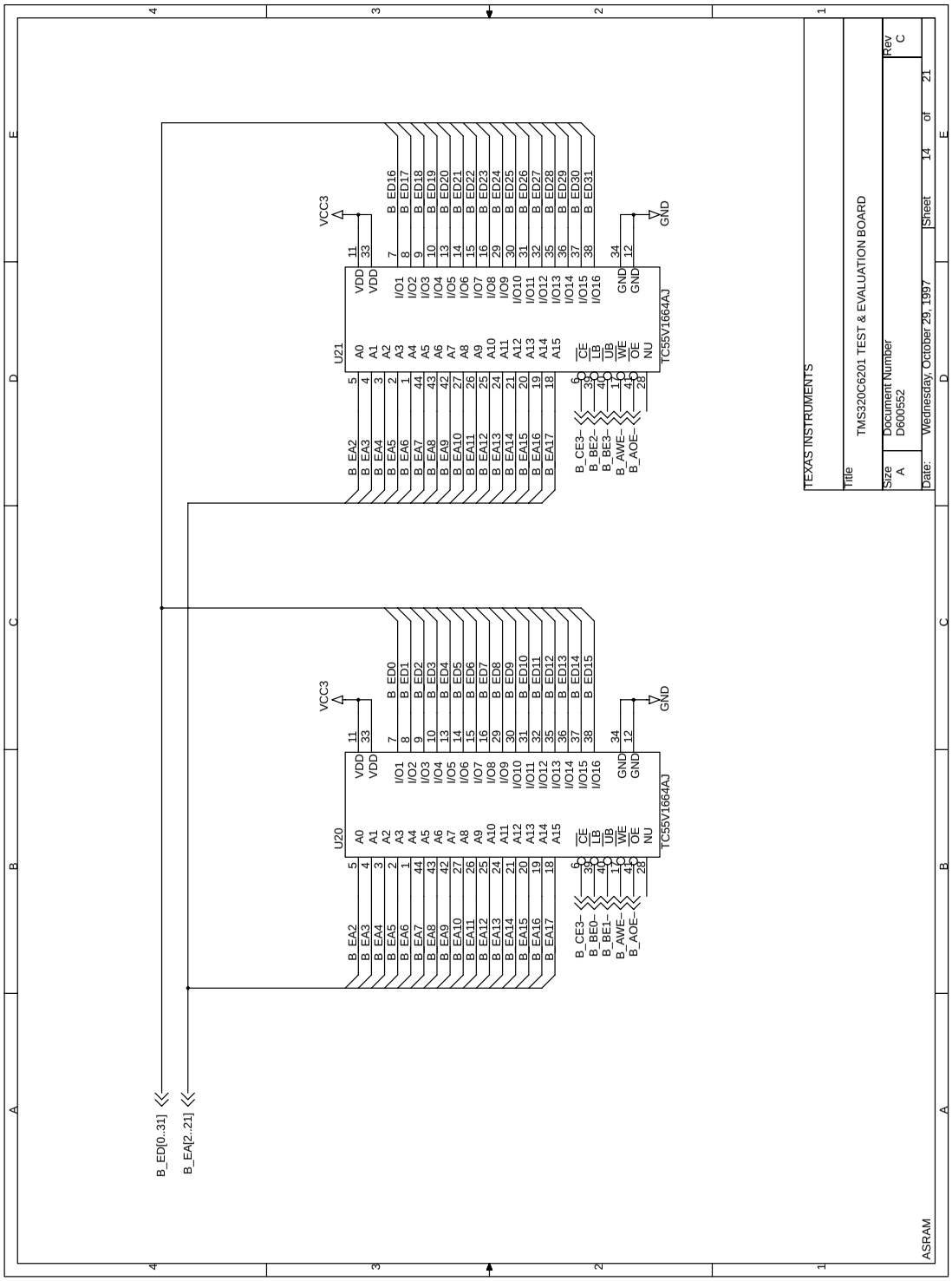
B_ED[0..31]
B_EA[2..21]
U20
U21
TC55V1664AJ
VCC3
GND
B_CE3–
B_BE0–
B_BE1–
B_BE2–
B_BE3–
B_AWE–
B_AOE–
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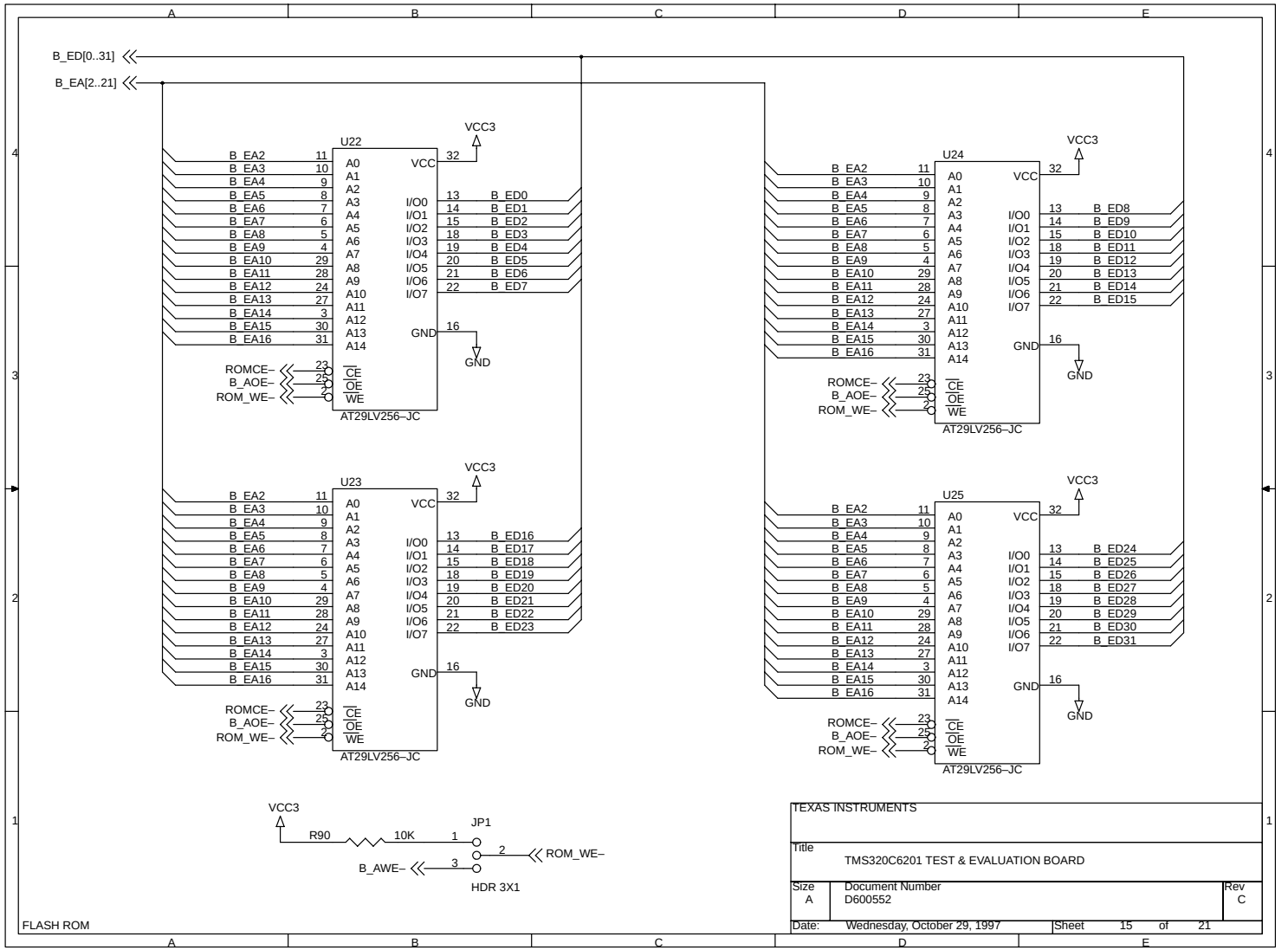
B_ED[0..31]
B_EA[2..21]
U22
U23
U24
U25
VCC3
GND
B_EA2
B_EA3
B_EA4
B_EA5
B_EA6
B_EA7
B_EA8
B_EA9
B_EA10
B_EA11
B_EA12
B_EA13
B_EA14
B_EA15
B_EA16
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
VCC
GND
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
B_ED0
B_ED1
B_ED2
B_ED3
B_ED4
B_ED5
B_ED6
B_ED7
B_ED8
B_ED9
B_ED10
B_ED11
B_ED12
B_ED13
B_ED14
B_ED15
B_ED16
B_ED17
B_ED18
B_ED19
B_ED20
B_ED21
B_ED22
B_ED23
B_ED24
B_ED25
B_ED26
B_ED27
B_ED28
B_ED29
B_ED30
B_ED31
ROMCE–
B_AOE–
ROM_WE–
CE
OE
WE
AT29LV256–JC
R90
10K
JP1
B_AWE–
HDR 3X1
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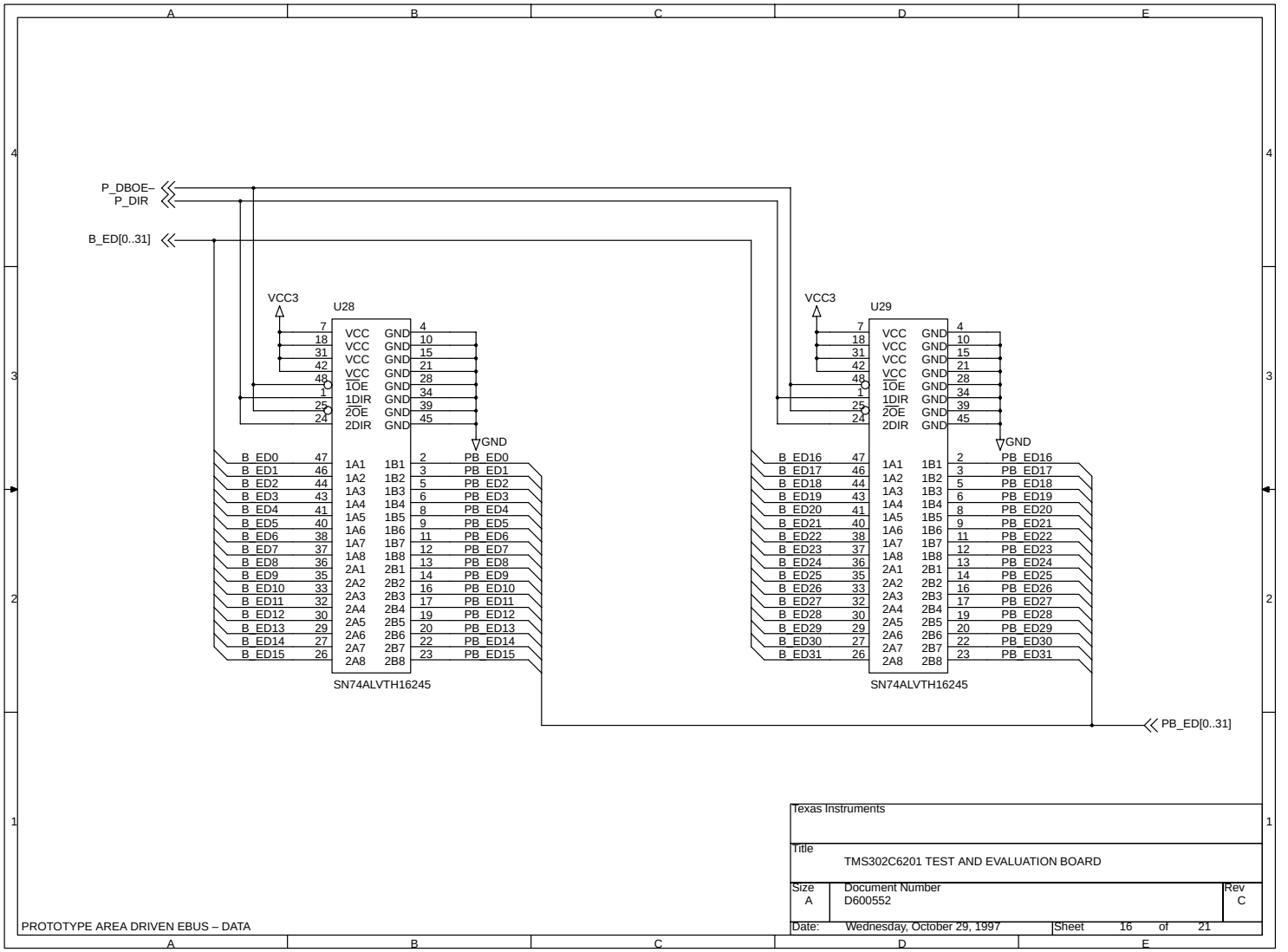
P_DBOE–
P_DIR
B_ED[0..31]
VCC3
U28
SN74ALVTH16245
B_ED0 B_ED1 B_ED2 B_ED3 B_ED4 B_ED5 B_ED6 B_ED7 B_ED8 B_ED9 B_ED10 B_ED11 B_ED12 B_ED13 B_ED14 B_ED15
PB_ED0 PB_ED1 PB_ED2 PB_ED3 PB_ED4 PB_ED5 PB_ED6 PB_ED7 PB_ED8 PB_ED9 PB_ED10 PB_ED11 PB_ED12 PB_ED13 PB_ED14 PB_ED15
VCC3
U29
SN74ALVTH16245
B_ED16 B_ED17 B_ED18 B_ED19 B_ED20 B_ED21 B_ED22 B_ED23 B_ED24 B_ED25 B_ED26 B_ED27 B_ED28 B_ED29 B_ED30 B_ED31
PB_ED16 PB_ED17 PB_ED18 PB_ED19 PB_ED20 PB_ED21 PB_ED22 PB_ED23 PB_ED24 PB_ED25 PB_ED26 PB_ED27 PB_ED28 PB_ED29 PB_ED30 PB_ED31
PB_ED[0..31]
PROTOTYPE AREA DRIVEN EBUS – DATA
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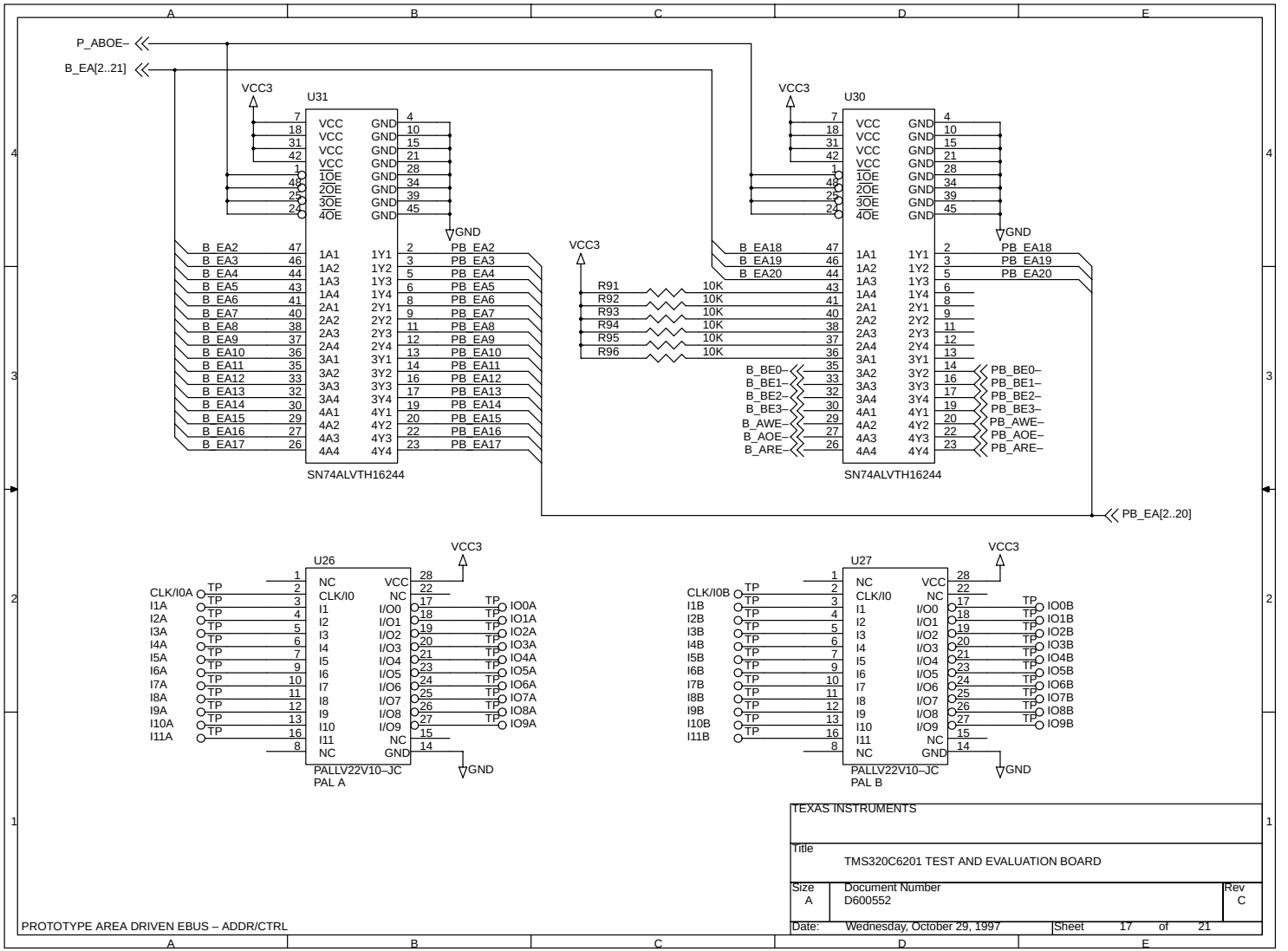
P_ABOE–
B_EA[2..21]
VCC3
U31
SN74ALVTH16244
B_EA2 B_EA3 B_EA4 B_EA5 B_EA6 B_EA7 B_EA8 B_EA9 B_EA10 B_EA11 B_EA12 B_EA13 B_EA14 B_EA15 B_EA16 B_EA17
PB_EA2 PB_EA3 PB_EA4 PB_EA5 PB_EA6 PB_EA7 PB_EA8 PB_EA9 PB_EA10 PB_EA11 PB_EA12 PB_EA13 PB_EA14 PB_EA15 PB_EA16 PB_EA17
U30
SN74ALVTH16244
B_EA18 B_EA19 B_EA20
PB_EA18 PB_EA19 PB_EA20
R91 R92 R93 R94 R95 R96 10K
B_BE0– B_BE1– B_BE2– B_BE3– B_AWE– B_AOE– B_ARE–
PB_BE0– PB_BE1– PB_BE2– PB_BE3– PB_AWE– PB_AOE– PB_ARE–
PB_EA[2..20]
U26
PALLV22V10–JC
PAL A
CLK/I0A I1A I2A I3A I4A I5A I6A I7A I8A I9A I10A I11A
IO0A IO1A IO2A IO3A IO4A IO5A IO6A IO7A IO8A IO9A
U27
PALLV22V10–JC
PAL B
CLK/I0B I1B I2B I3B I4B I5B I6B I7B I8B I9B I10B I11B
IO0B IO1B IO2B IO3B IO4B IO5B IO6B IO7B IO8B IO9B
GND
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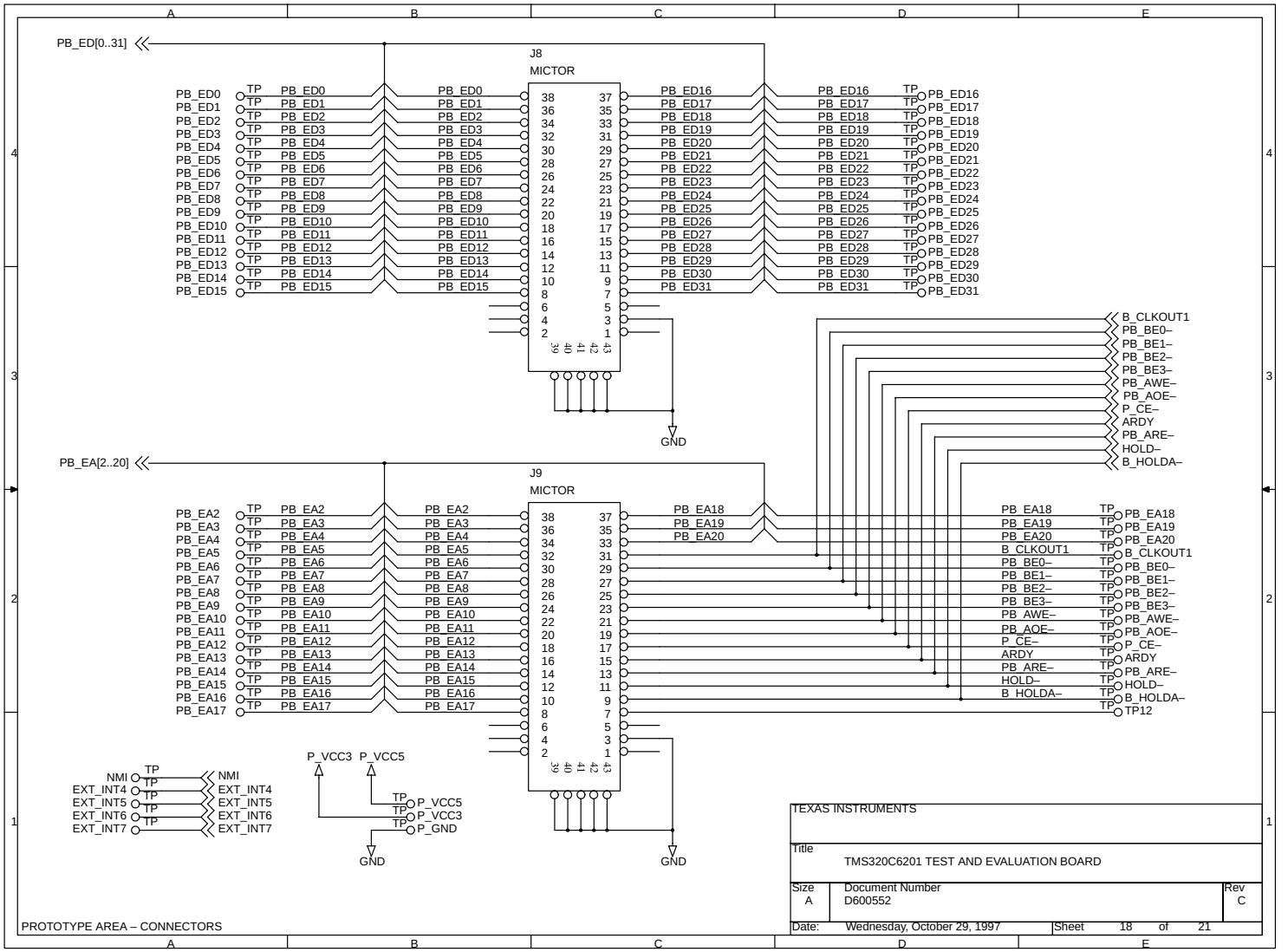
PB_ED[0..31]
J8
MICTOR
PB_ED0
PB_ED1
PB_ED2
PB_ED3
PB_ED4
PB_ED5
PB_ED6
PB_ED7
PB_ED8
PB_ED9
PB_ED10
PB_ED11
PB_ED12
PB_ED13
PB_ED14
PB_ED15
PB_ED16
PB_ED17
PB_ED18
PB_ED19
PB_ED20
PB_ED21
PB_ED22
PB_ED23
PB_ED24
PB_ED25
PB_ED26
PB_ED27
PB_ED28
PB_ED29
PB_ED30
PB_ED31
GND
PB_EA[2..20]
J9
MICTOR
PB_EA2
PB_EA3
PB_EA4
PB_EA5
PB_EA6
PB_EA7
PB_EA8
PB_EA9
PB_EA10
PB_EA11
PB_EA12
PB_EA13
PB_EA14
PB_EA15
PB_EA16
PB_EA17
PB_EA18
PB_EA19
PB_EA20
B_CLKOUT1
PB_BE0–
PB_BE1–
PB_BE2–
PB_BE3–
PB_AWE–
PB_AOE–
P_CE–
ARDY
PB_ARE–
HOLD–
B_HOLDA–
TP12
NMI
EXT_INT4
EXT_INT5
EXT_INT6
EXT_INT7
P_VCC3
P_VCC5
P_GND
TP
GND
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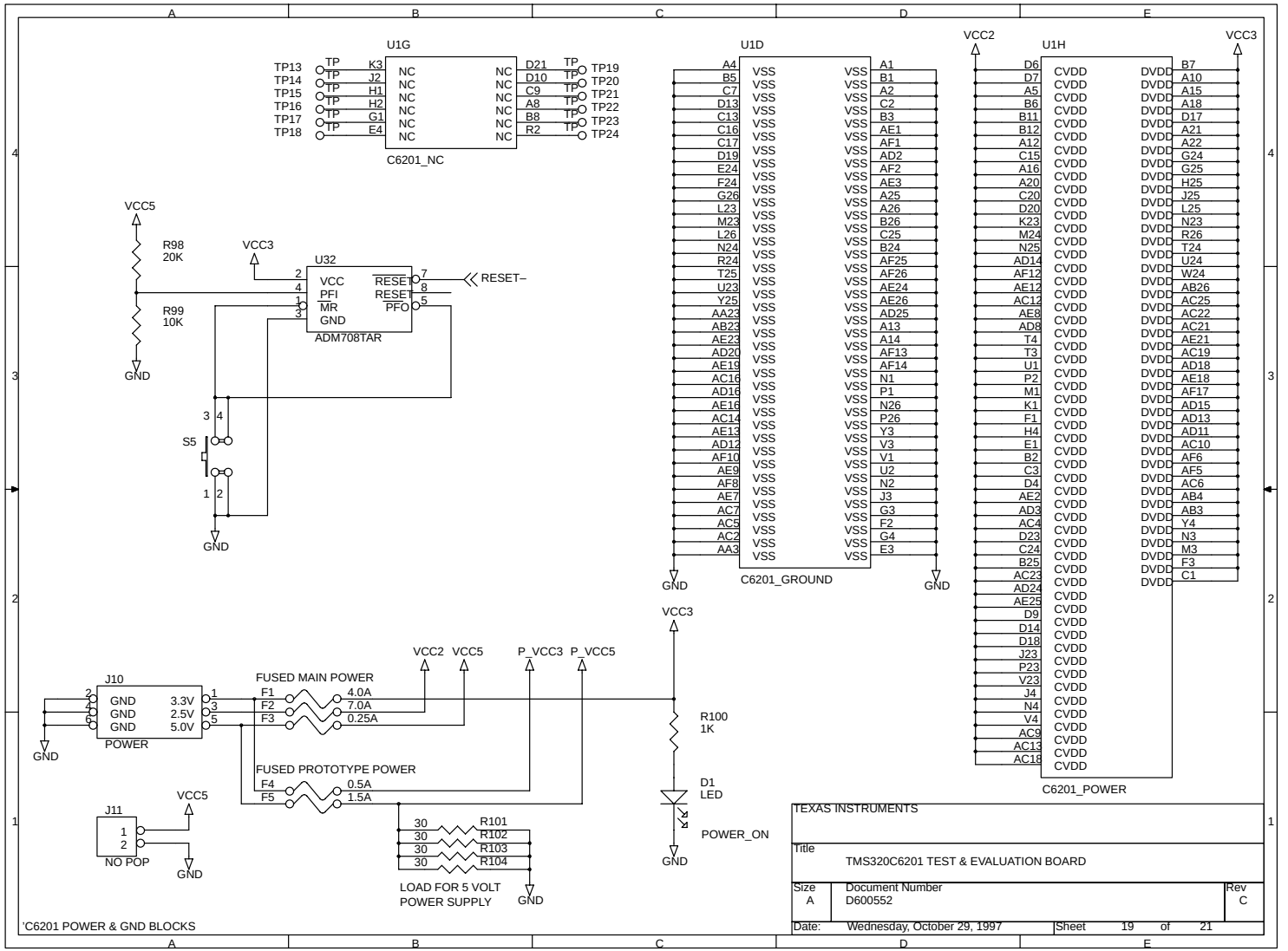
PROTOTYPE AREA – CONNECTORS


U1G
C6201_NC
U1D
C6201_GROUND
U1H
C6201_POWER
U32
ADM708TAR
RESET–
R98 20K
R99 10K
S5
J10
POWER
FUSED MAIN POWER
4.0A
7.0A
0.25A
FUSED PROTOTYPE POWER
0.5A
1.5A
J11
NO POP
R100 1K
D1 LED
POWER_ON
R101
R102
R103
R104
LOAD FOR 5 VOLT POWER SUPPLY
'C6201 POWER & GND BLOCKS
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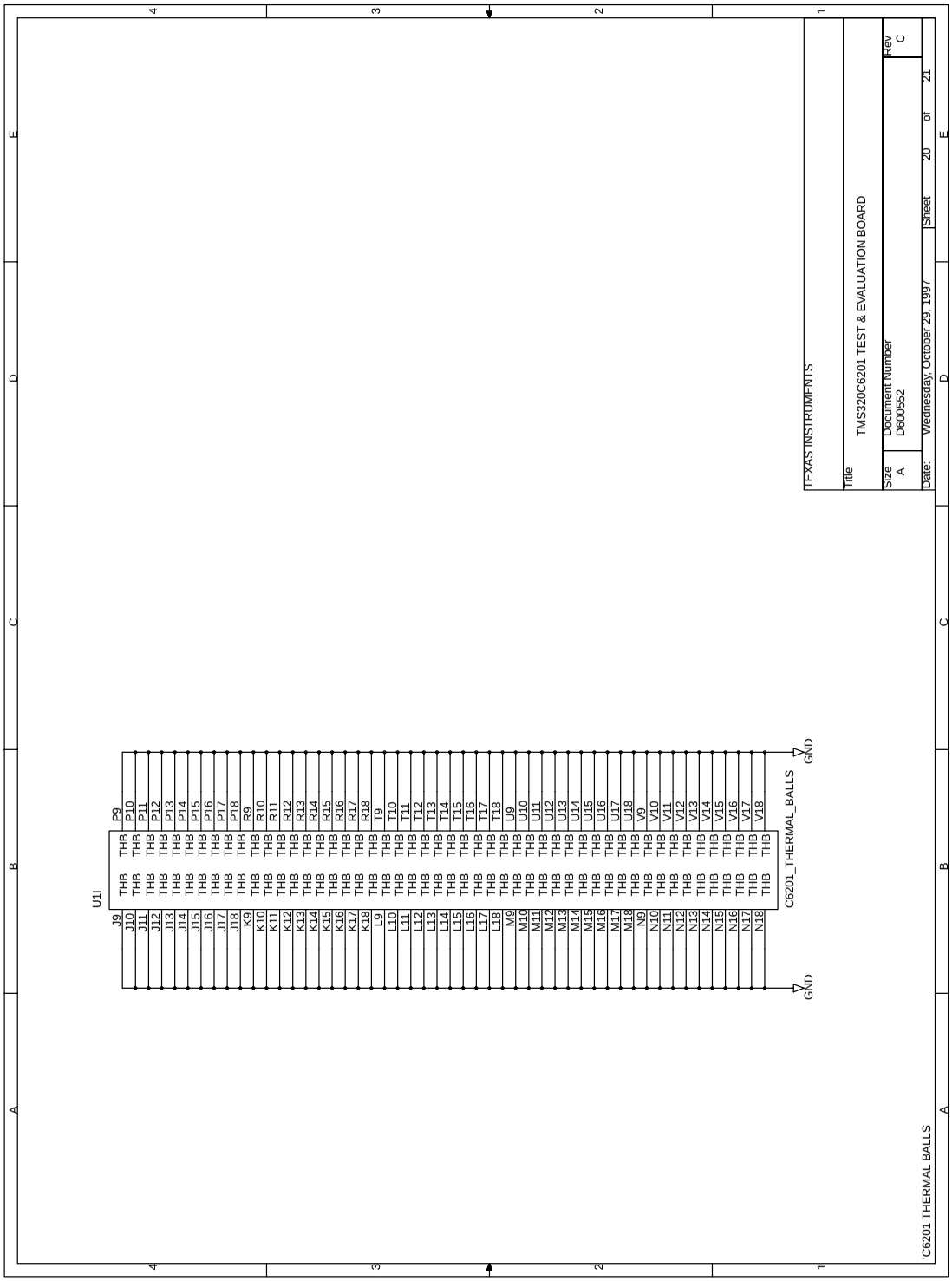
U1I
C6201_THERMAL_BALLS
GND
GND
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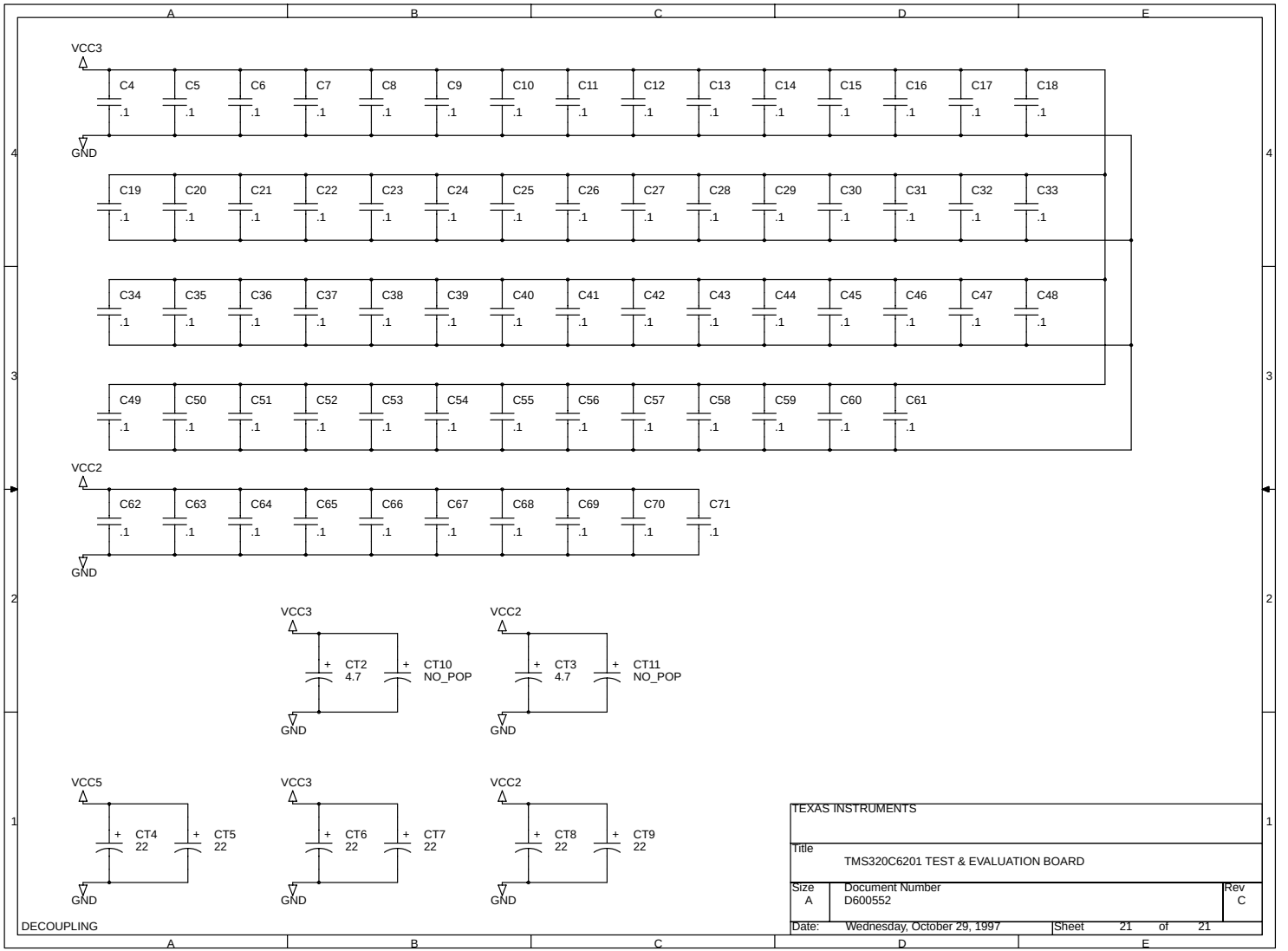
'C6201 THERMAL BALLS


VCC3
C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18
.1
GND
C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33
C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48
C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61
VCC2
C62 C63 C64 C65 C66 C67 C68 C69 C70 C71
CT2 4.7
CT10 NO_POP
CT3 4.7
CT11 NO_POP
VCC5
CT4 22
CT5 22
CT6 22
CT7 22
CT8 22
CT9 22
DECOUPLING
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